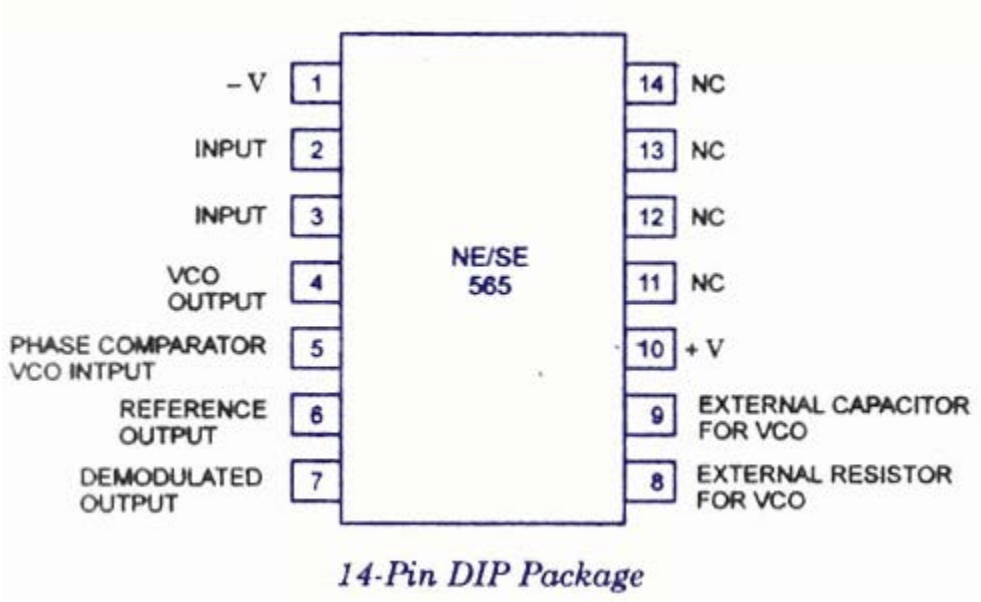
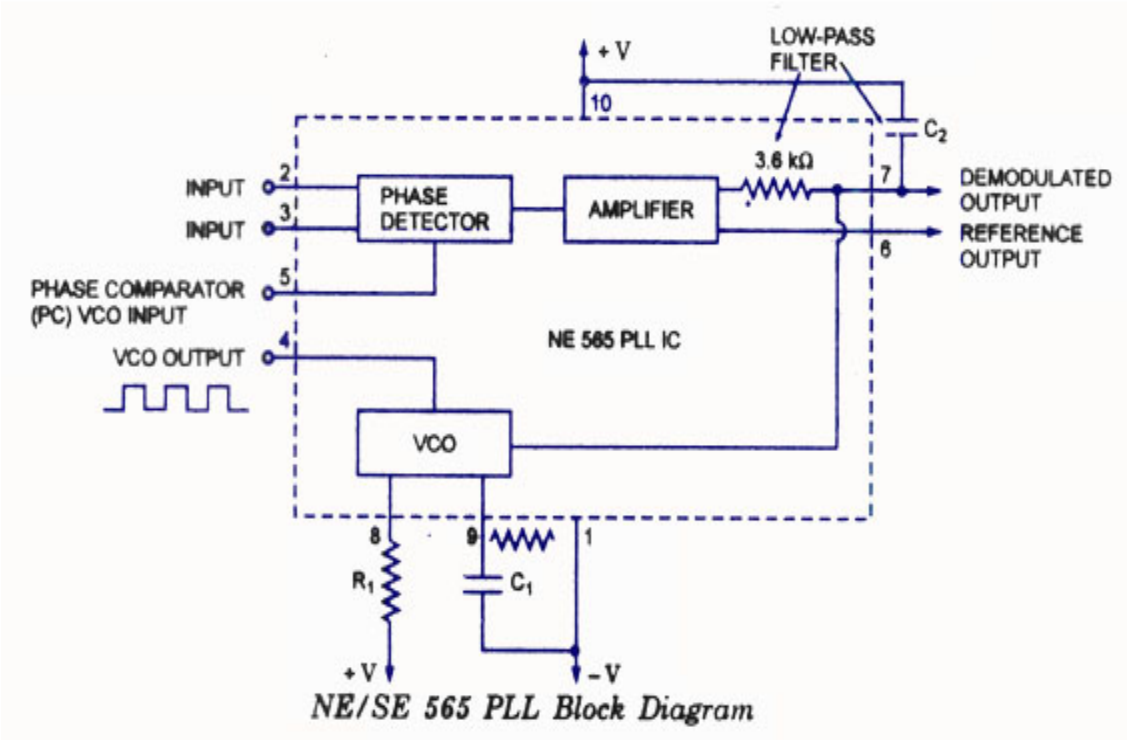
# MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565)

**Pin Configuration of PLL IC 565:**




*14-Pin DIP Package*

**Basic Block Diagram Representation of IC 565**




*NE/SE 565 PLL Block Diagram*

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA
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The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz----------(1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency $f_{OUT}$ is adjusted externally with R1 & C1 to be at the center of the input frequency range.
- C1 can be any value, R1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C2 connected between 7 & +V.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.
- The lock range $f_L$ & capture range fc of PLL is given by,

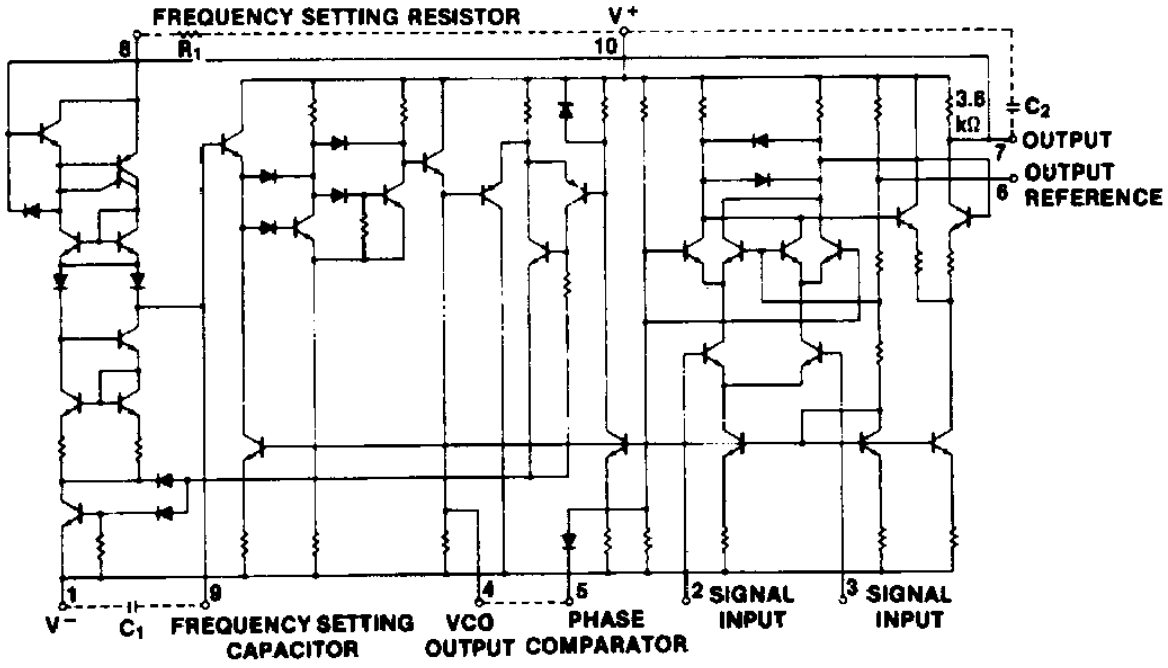
$$f_L = \pm \frac{8 \text{ fout}}{V} \text{ Hz ----------(2)}$$

Where $f_{OUT}$ = free running frequency of VCO (Hz)

V = (+V)-(-V) volts

$$f_C = \pm \left[ \frac{f_L}{(2\Pi)(3.6)(10^3)C_2} \right]^{½} \text{ ----------(3)}$$

**The circuit diagram of LM565 PLL**

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