MONOLITHIC PHASE LOCKED LOOP

PLL is now readily available as IC's which were developed in the SE/NE 560 series. Some of the commonly used ones are the SE/NE 560,561,562,564,565 and 567.The difference between each one of them is in the different parameters like operating frequency range, power supply requirements, and frequency and bandwidth ranges. Out of all the series the SE/NE 565 is the most famous. It is available as a 14-pin DIP and also as a 10-pin metal can package. The 14-pin DIP and its characteristics are given below.

Monolithic PLL Characteristics

- ⊡ Operating frequency range: 0.001 Hz to 500 kHz.
- ⊡ Operating voltage range: ± 6 to ± 12 V.
- ⊡ Input impedance: 10 k Q typically.
- ⊡ Output sink current: 1mA typically.
- ⊡ Output source current: 10 m A typically.
- ⊡ Drift in VCO centre frequency with temperature: 300 ppm/ °C typically.
- ⊡ Drift in VCO centre frequency with supply voltage: 1.5 %/V maximum.
- ⊡ Input level required for tracking: 10 mVrms minimum to 3 V peak-to-peak maximum.
- ⊡ Bandwidth adjustment range: < ± 1 to > ± 60 %.

The block diagram and connection diagrams are shown in the figure below.

The block diagram consist of a phase detector which acts as a phase comparator, an amplifier, and a low pass filter with the combination of the resistor (3.6 kilo ohm) and capacitor C2. The output of the amplifier is fed back to the VCO. The different pins representing that of the IC are also shown in the block diagram. Pins 1 and 10 are the positive and negative supply pins. The pins 2 and 3 are the input to the phase detector. The input signals are fed through these pins in differential mode. Pin 4 is the VCO output and pin 5 is the phase comparator VCO input. If both these pins are shorted the output of the VCO is supplied back to the phase comparator. The output of the phase comparator is given to the amplifier. The amplifier has two outputs that goes to the external pins as the demodulator output (pin 7) and the reference output (pin 6). An LPF circuit is formed by connecting the capacitor C2

between pin 7 and 10 with a resistor of value 3.6 kilo ohms. The value of C2 must be large enough to eliminate the variations in demodulated output and stabilize the VCO frequency.

Pins 8 and 9 are used to connect the external resistor (R1) and external capacitor (C1). The values of R1 and C1 help to adjust the free running frequency (fr) of the PLL. Though the value of C1 can be anything, the value of resistor R1 must have a value between 2 to 20 kilo ohms. All these factors can be used to determine the center frequency of the PLL.

The free running frequency of the PLL is given as fr = (1.2)/(4R1C1) Hertz

The lock range of the PLL is given as fLock = (+/-){(8fr)/V} Hertz

The capture range of PLL is given as fc = (fLock/[2* 10^3*C2])^1/2

The lock range usually increases with an increase in input voltage but falls with an increase in supply voltage.

Phase Locked Loop (PLL) – Working

Let us consider the free running frequency to be fr. Let fr be the frequency at which the Voltage Controlled Oscillator (VCO) is running without input signal. Let the input signal fi that is increasing from zero be applied to the phase comparator.

A graph between the error voltage and input frequency is shown below. It can be seen that when the input frequency is lesser than fi1,the error voltage Ver is reduced to zero. At this time the VCO will operate at the free running frequency, fr. When the input frequency, fi increases and reaches fi1, the error voltage jumps from zero to a negative voltage. This value will be equal to the difference between the input frequency and actual VCO output frequency (fi – fo).This resulting error voltage is then processed by filtering, amplifying, and applying the amplified voltage Vd to the control terminals of the VCO.

The instantaneous frequency of VCO decreases because fo falls for negative values of Vd and increases for positive values of Vrf. At some instant of time, the decreasing frequency of the VCO equals fin1 (lower edge of the capture range), then lock results-in, and the output signal frequency of the

VCO may be equal to the input signal frequency (that is, fo = fi). The VCO frequency locks with input signal frequency up to fi2 (the upper end of the lock range). If the input signal frequency exceeds fi2 then error voltage Vg will fall to zero and the VCO will operate at the free running frequency fr, as illustrated in figure. If the input signal frequency is now slowly swept back and it attains the value of fd1 then the loop (VCO frequency) locks with the input signal frequency, causing

a positive jump of the error voltage Ver. So the VCO output frequency increases from fr continuously till fo becomes equal to fi. The VCO frequency fo locks with the input signal frequency fi upto fd2 (the lower edge of the lock range) as shown in figure by dotted lines. Now if the frequency of the input signal falls below fd2, then the error voltage Ver will fall to zero and the VCO will operate at the free running frequency.

Source : http://www.circuitstoday.com/pll-phase-locked-loops#Monolithic-PLL