Mode S - Differential Phase shift Keying (DPSK)

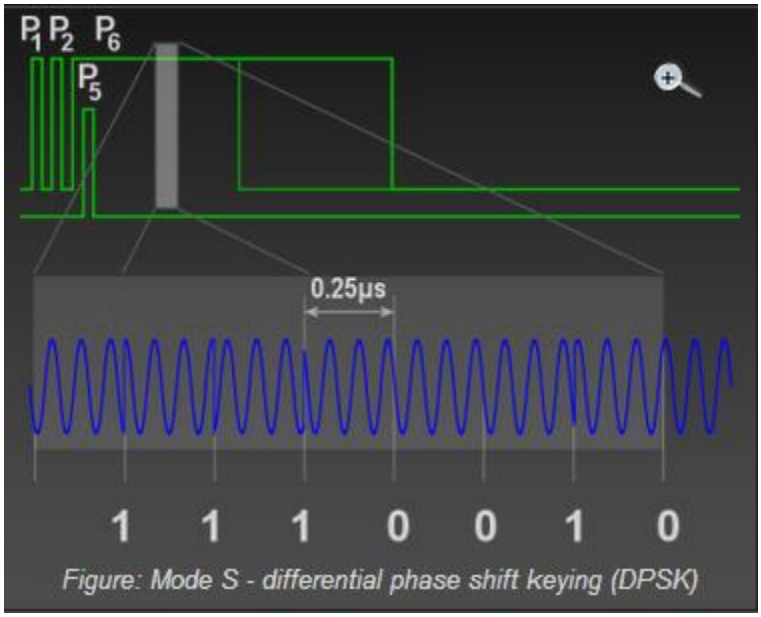

Figure: Mode S - differential phase shift keying (DPSK)

Mode S Uplink interrogations use into the P6 pulse Differential Phase Shift Keying (DPSK) to modulate the data in the uplink format. It is a type of phase modulation that conveys data by changing the phase of the carrier wave. All subsequent information in the P6 pulse is coded as 180° phase reversals of the carrier frequency. DPSK is a kind of phase shift keying which avoids the need for a coherent reference signal at the receiver. Each reversal must have a duration of 0.08 µs. Each received phase section has a duration of 0.25 µs and is known as a "chip" The DPSK decoder compares the phase between two consecutive chips and verify what the data must have been.

In ICAO Annex 10 Volume 4 is the interrogation data format described as follows: The interrogation data block shall consist of the sequence of 56 or 112 data chips positioned after the data phase reversals within P6. A 180-degree carrier phase reversal preceding a chip shall characterize that chip as a binary ONE. The absence of a preceding phase reversal shall denote a binary ZERO.

After the sync phase reversal all subsequent phase reversals indicate the 56 or 112 bit P6 information. All subsequent timing is taken from the point of the first phase reversal. The series of chips starts 0.5 µs after the sync reversal. At the end of P6 pulse there is a guard interval of 0.5 µs to ensure that distinct transmissions do not interfere with one another.

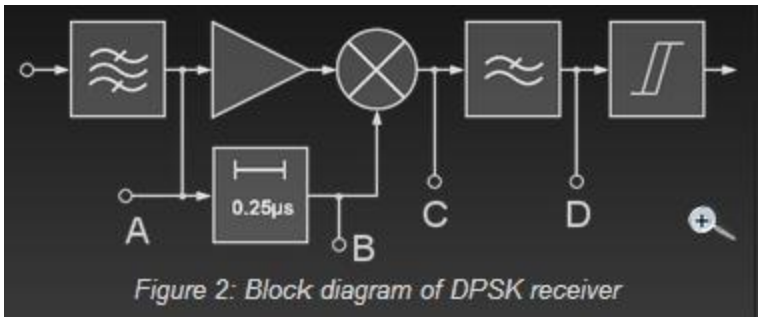

Figure 2: Block diagram of DPSK receiver

Whether the interrogation is short or a long pulse, the total duration of the P6 pulse is either 16.25 µs (56 data chips) or 30.25 µs (112 data chips). The P6 begins with an initial phase reversal at the start of the P6 pulse with a length of 1.25 µs. This is known as the sync phase reversal. To supress antenna sidelobes the pulse P5 is transmitted by an omnidirectional antenna. This pulse overlays the sync phase reversal and the transponder cannot decode the interrogation.

Figure 2 shows an evident option method of demodulation. At this DPSK decoder, the original sequence is recovered from the demodulated differentially encoded signal through a complementary process. The whole received signal is delayed for exact 0.25 microseconds. The origin and the delayed part will be compared. If the signals are in phase to each other, there is a lower output than if the phases (and the maximum amplitudes) have a contrary magnitude. From this output signal, the original serial bit pattern can be restored, which is indicated only by a low pass filter with the following threshold device.

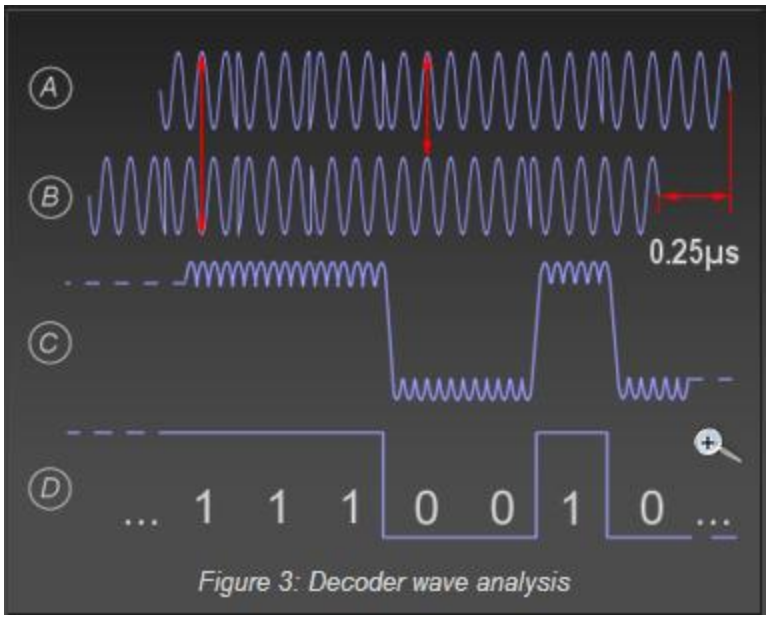

Figure 3: Decoder wave analysis

In Figure 3 the signal (C) at the output of the mixer is shown, formed by superposition of the delayed signal (B) and the undelayed original (A). An allocation of the output level to a bit can only be done, if by the synchronous phase reversal at the beginning of the P6 pulse triggers a counter to clock a shift register.

Source: http://www.radartutorial.eu/13.ssr/sr23.en.html