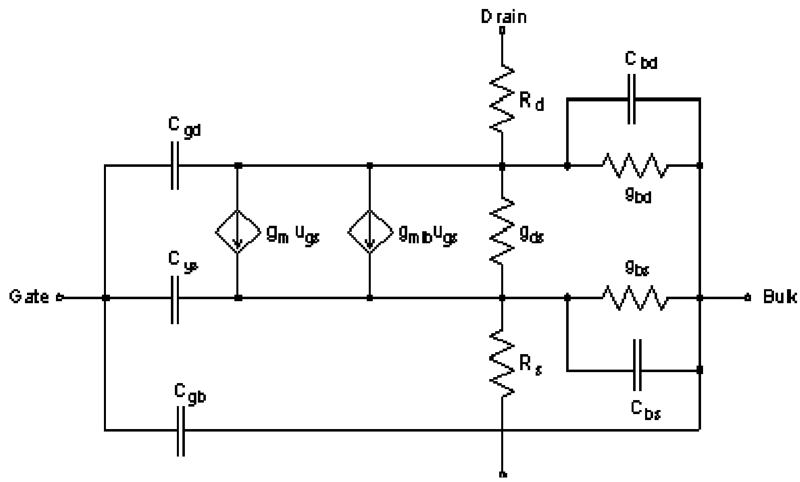
MOS TRANSISTOR CIRCUIT MODEL

These devices are known as FET's (Field effect transistors), which consist of three regions source, drain and gate. The resistance path between the drain and source is, controlled by applying a voltage to the gate. This varies the depletion layer under the gate and thus reduces or increases the conductance path. The FET input impedance (unlike the BJT which is a few KΩ) is very high (~MΩ's) and as a result the gate current can be considered as zero.



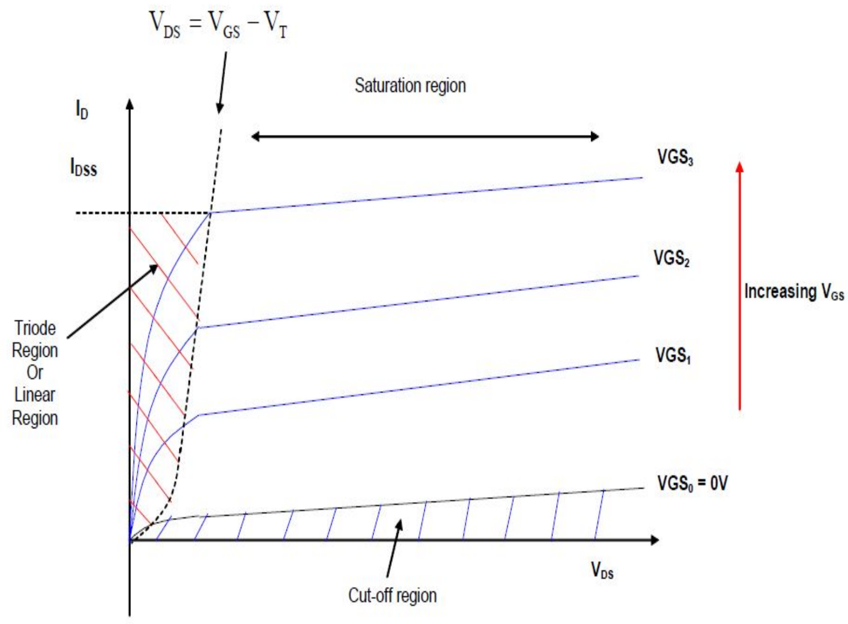


Fig. 8 MOS Transistor Circuit Model

As per the BJT the FET is best described by it's Output I-V DC characteristics (N-type enhancement characteristics shown below), however things are complicated by the fact there are two types of FET depletion and enhancement that are both available as N-type or P-type devices. For low frequencies the enhancement devices are more commonly used (Depletion mode types will be described when discussing microwave devices).

(1) Cut-Off Region – In this region the gate voltage is less than the pinch-off voltage Vp and therefore very little current flows.

(2) Triode Region – In this mode the device is operating below pinch-off and is effectively a variable resistor. R_{OUT} is ~ linear but only over a small range of V_{DS}.

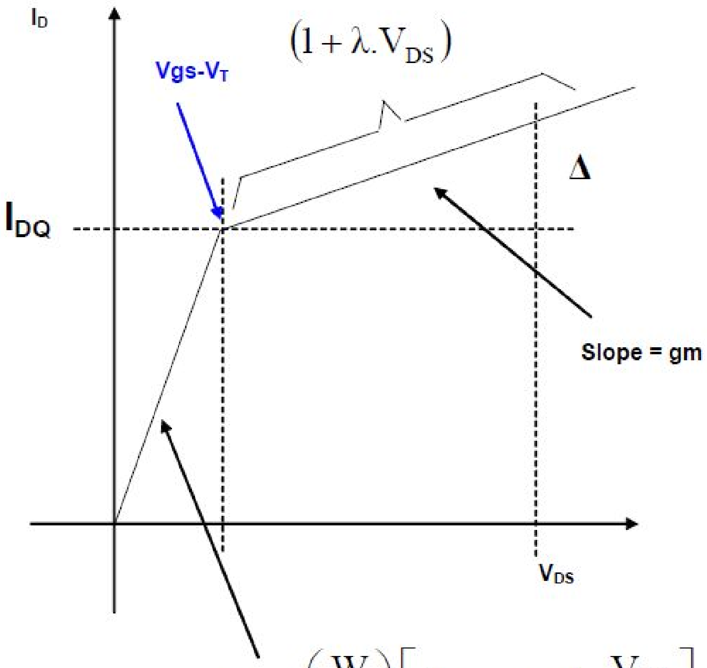
(3) Saturation Region – This is the main operating region for the device. The drain voltage has to be greater than the gate voltage less the pinch-off voltage – this sets the minimum supply voltage. The curves in the saturation region can be extrapolated to a point 1/λ, where λ is known as the 'Channel length modulation parameter, (units V^{-1}), - this is analogous to the BJT Early voltage.

$$I_D = I_{DQ} + \Delta$$

$$I_{DQ} + G_O.V_{DS}$$

$$I_{DS} + \lambda.I_{DS}.V_{DS}$$

$$= I_{DS}.(1 + \lambda.V_{DS})$$



$$\mu_O.C_{OX}.\left(\frac{W}{L}\right).\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right].V_{DS}$$

$$ID = \mu_O.C_{OX}.\left(\frac{W}{L}\right).\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right].V_{DS}(1 + \lambda.V_{DS})$$

Non saturation/ non linear region only

Where μ_O = Surface mobility of device

$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$ = capacitance per unit area of gate oxide

W = Effective channel width

L = Effective channel length

W/L = Known as the aspect ratio

VT = Device threshold voltage

λ = Channel length modulation parameter

For saturation region ie $V_{DS} > (V_{GS}-V_T)$

$$I_D = \beta[V_{GS} - V_T]^2(1 + \lambda.V_{DS})$$

Where $\beta = \frac{\mu_O.C_{OX}\left[\frac{W}{L}\right]}{2}$ Known as the transconductance parameter

$$I_D \approx \beta[V_{GS} - V_T]^2$$

Source : http://msk1986.files.wordpress.com/2013/09/7ec5-vlsi-design-unit-1-notes.pdf