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Low Power VLSI Techniques Using Booth Algorithm for Digital Filter for Hearing aid Applications

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Abstract- In the past few years there has been an explosive growth in the demand for portable computing and communication devices, from mobile telephones to sophisticated multimedia systems. This interest in these devices has enhanced the requirement of developing low-power signal processors and algorithms, as well as the development of low-power general purpose processors. Designers have been able to reduce the energy requirements of particular functions, such as video compression, by several orders of magnitude. This reduction has come as a result of focusing on the power dissipation at all levels of the design process, from algorithm design to the detailed implementation, however, there has been little work done to understand how to design energy efficient processors.[1][2] .

Keywords-**Booth Multiplier, Booth Wallace Multiplier, Digital filters, MAC Unit.**

I. INTRODUCTION

In add and shift algorithm the initial partial product is taken as zero. In each step of the algorithm, LSB bit of the multiplier is tested, discarding the bit which was previously tested, and hence generating the individual partial products. These partial products are shifted and added at each step and the final product is obtained after n steps for n x n multiplication. The main disadvantage of this algorithm is that it can be used only for unsigned numbers. The range of the input for a 'n' bit multiplication is from 0 to 2n-1. A better algorithm which handles both signed and unsigned integers uniformly is Booth's algorithm. Booth encoding is a method used for the reduction of the number of partial products proposed by A.D. Booth in 1950.[12]

X=-2mXm + 2m-1 Xm-1 + 2m-2 Xm-2+…….

Rewriting above equation using 2a=2 a+1 - 2a leads to X=-2m(Xm-1–Xm)+2m-1(Xm-2+Xm-1)+2m-2(Xm-3-Xm-2)Considering the first 3 bits of X, we can determine whether to add Y, 2Y or 0 to partial product. The grouping of X bits is shown in figure 1[4].

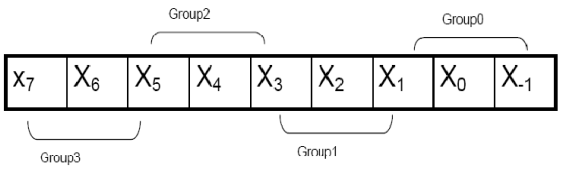

Fig.1.Multiplier bit grouping according to Booth encoding [14]

The multiplier X is segmented into groups of three bits (Xi+1, Xi, Xi-1) and each group of bits is associated with its own partial product row using table 1[3], [14].

Table 1. Booth encoding [3]

X_{i+1}	X_i	X_{i-1}	Increment
0	0	0	0
0	0	1	Y
0	1	0	Y
0	1	1	2Y
1	0	0	-2Y
1	0	1	-Y
1	1	0	-Y
1	1	1	0

Booth's algorithm [9] is based on the fact that fewer partial products have to be generated for groups of consecutive '0' in the multiplier there is no need to generate any new partial product. For every '0' bit in the multiplier, the previously accumulated partial product needs only to be shifted by one bit to the right. The above can be implemented by recoding the multiplier as shown in the table 2[5].

Pipelined Modified Booth Multiplier: A pipelined modified Booth multiplication is proposed to enhance the power performance ratio of 2's complement multiplication. System architecture of the proposed scheme is catered for VLSI implementation. It is designed with the merit of low power consumption achieved by reducing the number of adder required. Only half of the adders is required as in traditional pipelined multiplier. Modified Booth algorithm is widely used to implement multiplication in DSP systems and other applications. It provides high performance than other multiplication algorithms. However, the intrinsic architecture

of the modified Booth algorithm does not have the regularity for VLSI pipeline implementation.

Table 2-Multiplier recoding for radix-4 booth's algorithm [14]

Sl. No.	mr_{i+1}	mr_i	mr_{i-1}	Recoded digit	Operation on multiplicand
1	0	0	0	0	0 X Multiplicand
2	0	0	1	+1	+1 X Multiplicand
3	0	1	0	+1	+1 X Multiplicand
4	0	1	1	+2	+2 X Multiplicand
5	1	0	0	-2	-2 X Multiplicand
6	1	0	1	-1	-1 X Multiplicand
7	1	1	0	-1	-1 X Multiplicand
8	1	1	1	0	0 X Multiplicand

For power reduction, reducing the supply voltage is widely used to improve the system power efficiency. It is most effective in pipelined data path comparing to other implementations such as parallel data path and pipeline-parallel data path. For reduction of power and supply voltage, pipelined data path is being widely used in DSP systems to enhance the system throughput. In the paper [7], we proposed a pipelined modified Booth multiplication to improve the system performance in terms of system throughput and power-performance ratio for low power low voltage DSP applications.

Problems in computing 2's complement number: Multiplying two numbers, *X* (multiplicand) and *Y* (multiplier), Booth algorithm encodes the two's complement multiplier, Y, to reduce the number of partial products to be added. The Radix - 4 modified Booth algorithm [8] divides the multiplier into overlapping groups of 3-bit encoded into {-2,-1, 0, 1, 2}. Each group is decoded to generate the partial product.

II. PROPOSED MAC

If an operation to multiply two N-bit numbers and accumulate into a 2N-bit number is considered, the critical path is determined by the 2N-bit accumulation operation. if a pipeline scheme is applied for each step in the standard design of Fig ,the delay of last accumulator must be reduced in order to improve the performance of the MAC. The overall performance of the proposed MAC is improved by eliminating the accumulator itself by combing it with CSA function. if the accumulator has been eliminated, the critical path is then determined by the final adder in the multiplier .The basic method to improve the performance of final adder is to decrease the no of input bits. In order to reduce these no input bits, the multiple partial products are compressed into a sum and carry by CSA .the number of bits of sums and carries to be transferred to the final adder is reduced by adding lower bits of sums and carries in advance with in the range in which the overall performance will not be degraded.

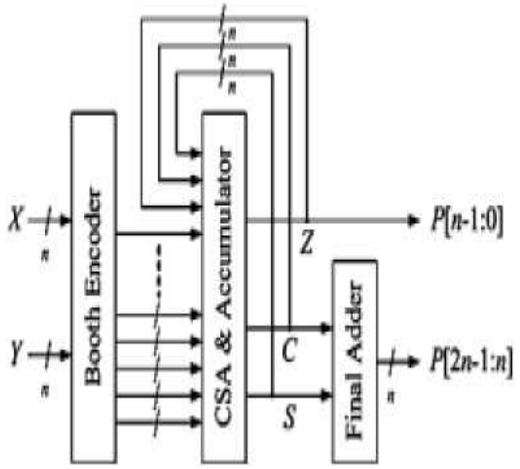

Fig.2. Hardware Architecture MAC [11]

III. MODIFIED BOOTH 'S ALGORITHM [11]

Multiplication consists of three steps: 1) the first step to generate the partial products; 2) the second step to add the generated partial products until the last two rows are remained; 3) the third step to compute the final multiplication results by adding the last two rows. The modified Booth algorithm reduces the number of partial products by half in the first step. We used the modified Booth encoding (MBE) scheme proposed in. It is known as the most efficient Booth encoding and decoding scheme. To multiply X by Y using the modified Booth algorithm starts from grouping Y by three bits and encoding into one of {-2, -1, 0, 1, 2}. Table I shows the rules to generate the encoded signals by MBE scheme.

Spurious Power Suppression Technique [11]: 16-bit adder/subtractor design example based on the proposed SPST. In this example, the 16-bit adder/subtractor is divided into MSP and LSP at the place between the 8th bit and the 9th bit. Latches implemented by simple AND gates are used to control the input data of the MSP. When the MSP is necessary, the input data of MSP remain the same as usual, while the MSP is negligible, the input data of the MSP become zeros to avoid switching power consumption.

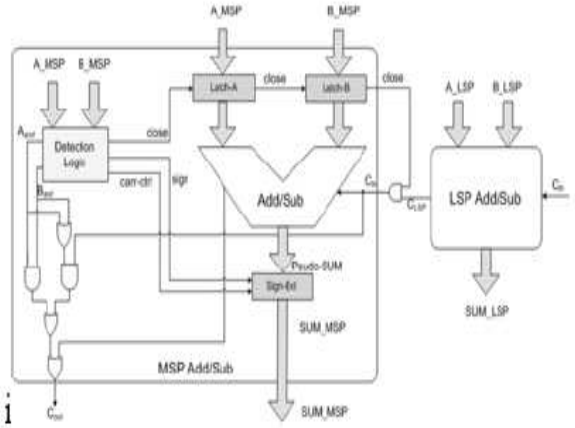

Fig.3. 16-bit adder/subtractor design [11]

IV. CONCLUSION

Booth Algorithm is used for Low Power VLSI Techniques for Digital Filter for Hearing aid applications. Various types of multiplication & accumulation techniques are used for booth multiplier & booth Wallace tree multiplier. A RADIX-4 Modified Booth multiplier circuit is used for MAC architecture. Compared to other circuits, the Booth multiplier has the highest operational speed and less hardware count. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. Power and delay is calculated for the blocks. The power reduction techniques adopted in this work. The MAC unit designed in this work can be used in filter realizations for High speed DSP applications.

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