LIBRARIES IN PHYSICAL DESIGN

Technology libraries are integral part of the ASIC backend EDA tools. Important two libraries are briefly explained below.

Technology File Libraries

Technology file defines basic characteristic of cell library pertaining to a particular technology node. They are units used in the design, graphical characteristics like colors, stipple patterns, line styles, physical parameters of metal layers, coupling capacitances, capacitance models, dielectric values, device characteristics, design rules. These specifications are divided into technology file sections.

Units for power, voltage, current etc are defined in technology section.

The color section defines primary and display colors that a tool uses to display designs in the library.

Stipple pattern are defined in stipple sections.

Different layer definitions like its current density, width etc are defined in layer section.

Fringe capacitances generated by crossing of interconnects are defined in fringe cap section.

Similarly several other specifications like metal density, design rules that apply to design in library, place and route (P&R) rules, slot rule, resistance model are defined in their respective sections.

Standard Cell Libraries, I/O Cell Libraries, Special Cell Libraries

A standard cell library is a collection of pre designed layout of basic logic gates like inverters, buffers, ANDs, ORs, NANDs etc.

All the cells in the library have same standard height and have varied width. These standard cell libraries are known as ***reference libraries in Astro***.

These reference libraries are technology specific and are generally provided by ASIC vendor like TSMC, Artisan, IBM etc. Standard cell height for 130 TSMC process is 3.65 µM.

In addition to standard cell libraries, reference libraries contain I/O and Power/Ground pad cell libraries. It also contain IP libraries for reusable IP like RAMs, ROMs and other pre-designed, standard, complex blocks.

The TSMC universal I/O libraries include several power/ground cells that supply different voltages to the core, pre-drivers and post drivers. Internal pull-up or pull-down is provided to some cells in I/O libraries.

Source : http://asic-soc.blogspot.in/2007/10/libraries-in-physical-design.html