Abstract:
Power and delay are two main constraints in ASIC design. Trying to optimize the design with respect to power might result in an increase in the delay. This trade-off between power and delay are analyzed in this paper. In this design both mixed vt and clock gating techniques (mixed design) are used to reduce power. The TDES block is Place and Routed using SoC Encounter by using the above mentioned mixed design methodology. Therefore by analyzing the power delay tradeoff we suggest the best technique for TRIDES MAC block is the mixed design method.

Keywords: ASIC, TDES ,STA, CTS. Multi vt.

1. Introduction

Power consumption awareness began worldwide around 1990–1992. Before that, only niche markets required low-power integrated circuits (ICs). Today, every circuit has to face the power consumption issue, for both portable devices aiming at longer battery life and high-end circuits avoiding cooling packages and reliability issues that are too complex.

Physical design is an important process among a lot of processes followed in chip design. Physical design is an important process in ASIC design which defines to Physical synthesis (i.e.) implementing from optimized gate level net-list to GDSII stream-out data. Major Constraints of Physical design is Timing, Power and Area. Period for improving electronic circuits have been rediscovered and reused in the last 10 years, focusing on power consumption reduction.

Today’s connected society pervasively uses the data encryption. The two most basic facts of modern day data encryption are data privacy and authentication. As modern society becomes more connected, and more information becomes available there is a need for safeguards which bring data integrity and data secrecy. In
addition, authenticating the source of information gives the recipient, with complete certainty that the information came from the original source and that it has not been altered from its original state. Both, the needs for information privacy and data authentication has motivated cryptography. Of the several data encryption types, Data Encryption Standard (DES) and its variant Triple-DES (TDES) Fig.1 have emerged to be the most commonly used in varying applications. All the simulations have been done on Cadence Soc Encounter version 10.1.

2. ASIC Design Flow

ASIC is a combination of digital and analog circuits packed into an IC to achieve the desired control/computation function Initial target of an IC is to have programmable devices to adapt to various functions (e.g., Microprocessor systems like 8051, 8086 etc.) . Fig. 2 shows the ASIC Physical Design (PD) flow.

![Fig.2. ASIC design flow](image-url)
3. Experimental Results

3.1. Floor planning

Floor planning (Fig.3) is an important step in ASIC Physical Design. Here we go with a utilization factor of 0.7. A detailed description about how to choose an optimal Utilization factor is given in [1]. All the core margins are set to 1 micron from all the four sides.

![Floor planning specification](image1)

Fig. 3 Floor planning   Specification

3.2. Power planning

Here we use a 8 metal layer process. Here both horizontal and vertical power stripes are laid as the design is standard cell intensive. The seventh (horizontal layer) layer is used for the horizontal stripes and the eighth (vertical layer) layer is used for the vertical stripes. Fig. 4 shows the power planning.

![Power planning](image2)

Fig.4. power planning

3.3. Placement

Placement of the standard cells with S-Route is done and the congestion is checked. If the congestion is less than 0.5% of the total G cell count, we proceed to the next step. Fig. 5 shows the placement of standard cells.
3.4. Trail Route

Trial route is type of global routing in which the nets are routed with strainer lengths. It is done in order to get the initial timing reports. Fig.6 shows the trial routed chip.

3.5. Clock tree synthesis

CTS is the process in which we make sure that the clock is reaching all the flops with the same insertion delay and with the same transition time. Here we have used two clock inverters with strength 8x and 12x to build the clock tree. Fig.7 shows the chip with the clock tree built.
3.6. Post Route

After building the clock tree we go for the actual routing i.e detailed routing. This routing is both timing and SI (Signal Integrity) driven. After doing the final route and after fixing all the setup and hold violations the final reports are shown below. Note that we only fix hold in the post route stage. Fig. 8 and Fig 9 shows the results after post route stage.

```
timeDesign Summary

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<tr>
<th></th>
<th>all</th>
<th>reg2reg</th>
<th>in2reg</th>
<th>reg2out</th>
<th>in2out</th>
<th>clkgate</th>
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<tbody>
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<td>1.602</td>
<td>8.026</td>
<td>1.745</td>
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<tr>
<td>TNS (ns):</td>
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<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
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<tr>
<td>Violating Paths:</td>
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<td>0</td>
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<td>805</td>
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<td>1</td>
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<table>
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<th>Real</th>
<th>Total</th>
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<td>Worst Viol</td>
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<td>0 (0)</td>
<td>0.000</td>
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<tr>
<td>max_fanout</td>
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Density: 60.466%```

Fig.8. post route for set up

```
timeDesign Summary

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<th>Hold mode</th>
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<th>in2reg</th>
<th>reg2out</th>
<th>in2out</th>
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<td>TNS (ns):</td>
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<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>Violating Paths:</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>All Paths:</td>
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<td>41938</td>
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<td>1</td>
<td>149</td>
</tr>
</tbody>
</table>

Density: 60.466%```

Fig.9. post route for hold

4. Low Power Simulation Results

Here we have used both Multi vt optimization technique (for reducing leakage power) and Clock Gating technique (for reducing dynamic power). The results are shown in Fig. 10 and Fig. 11.
5. Conclusion

At each stage in the ASCI PD flow we observe that the density increases and new timing violations are observed. This project is implemented using the timing driven placement in the tool. Almost 50% power reduction has been achieved. By using the Low power techniques. Here we can implement in the 65nm. In future we can implement 22nm and achieve less power and less in area.

References

[9] www.soccentral.com
[10] www.cadence.com

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