INVERTER DELAYS, CMOS INVERTER AND FORMAL ESTIMATION OF DELAY

We have seen that the inverter is associated with pull up and pull down resistance values. Specially in nmos inverters. Hence the delay associated with the inverter will depend on whether it is being turned off or on. If we consider two inverters cascaded then the total delay will remain constant irrespective of the transitions. Nmos and CMOS inverter delays are shown next.

NMOS INVERTER

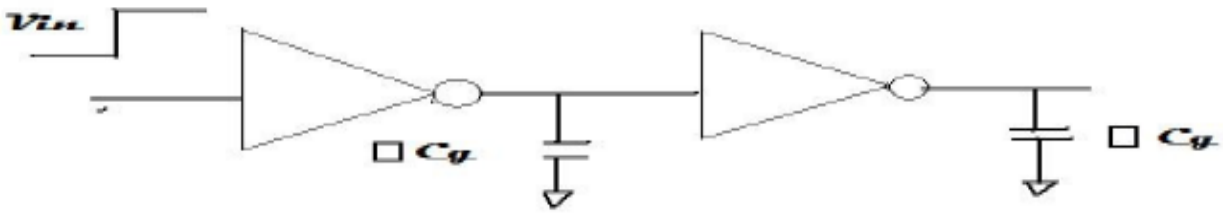

Figure 8: Cascaded nmos inverters.

Let us consider the input to be high and hence the first inverter will pull it down. The pull down inverter is of minimum size nmos. Hence the delay is 1□. Second inverter will pull it up and it is 4 times larger, hence its delay is 4□.The total delay is 1□ +4□= 5□. Hence for nmos the delay can be generalized as T=(1+Zpu/Zpd) □

CMOS INVERTER:

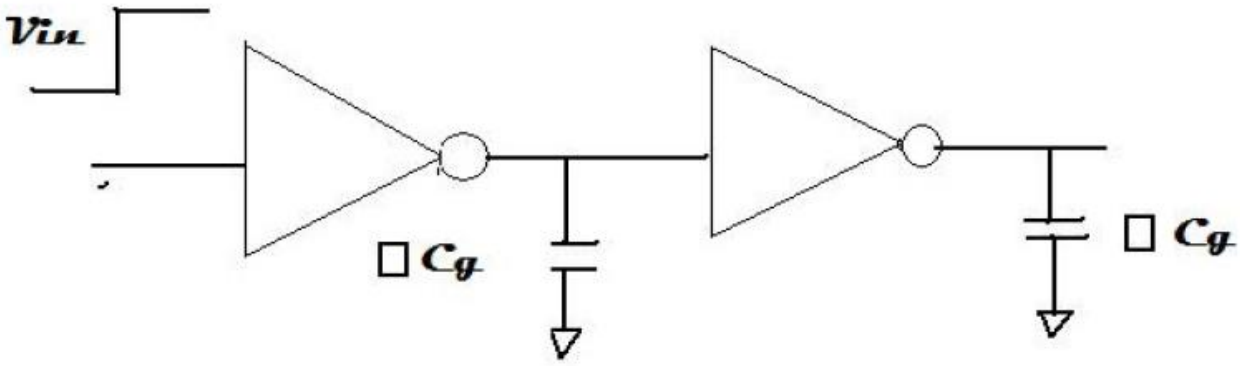

Figure 9: Cascaded CMOS inverter.

Let us consider the input to be high and hence the first inverter will pull it down. The nmos transistor has Rs = 10k and the capacitance is 2Cg. Hence the delay is 2□. Now the second inverter will pull it up, job done by the pmos. Pmos has sheet resistance of 25k i.e 2.5 times more, everything else remains same and hence delay is 5□. Total delay is 2□ +5□ = 7□ . The capacitance here is double because the input is connected to the common poly, putting both the gate capacitance in parallel. The only factor to be considered is the resistance of the p gate which is increasing the delay. If want to reduce delay, we must reduce resistance. If we increase the width of p channel, resistance can be reduced but it increases the capacitance. Hence some trade off must be made to get the appropriate values.

FORMAL ESTIMATION OF DELAY

The inverter either charges or discharges the load capacitance CL. We could also estimate the delay by estimating the rise time and fall time theoretically.

Rise time estimation

Assuming that the p device is in saturation we have the current given by the equation Idsp=ßp(Vgs-|Vtpl)2/2

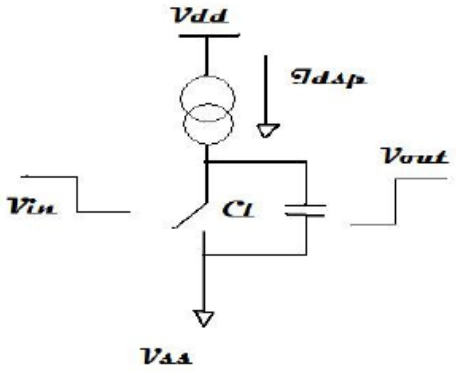

Figure 10: Rise time estimation.

The above current charges the capacitance and it has a constant value therefore the model can be written as shown in figure above. The output is the drop across the capacitance, given by

Vout =Idsp x t/CL

Substituting for Idsp we have Vout=ßp(Vgs-|Vtpl)2t/2CL. Therefore the equation for t=2CLVout/ßp(Vgs-|Vtpl).Let t=□r and Vout=Vdd, therefore we have □r = 2VddCL/ßp(Vgs-|Vtpl)2. If consider Vtp=0.2Vdd and Vgs=Vdd we have □r = 3CL/ßpVdd

On similar basis the fall time can be also be written as □f = 3CL/ßnVdd whose model can be written as shown next