# Internal 8253 Registers

Here is a list of the internal 8253 registers that will program the internal counters of the 8253:

| | RD | WR | A0 | A1 | function |
|---|---|---|---|---|---|
| COUNTER 0 | 1 | 0 | 0 | 0 | Load counter 0 |
| | 0 | 1 | 0 | 0 | Read counter 0 |
| COUNTER 1 | 1 | 0 | 0 | 1 | Load counter 1 |
| | 0 | 1 | 0 | 1 | Read counter 1 |
| COUNTER 2 | 1 | 0 | 1 | 0 | Load counter 2 |
| | 0 | 1 | 1 | 0 | Read counter 2 |
| MODE WORD or CONTROL WORD | 1 | 0 | 1 | 1 | Write mode word |
| - - | 0 | 1 | 1 | 1 | No-operation |

**Counter #0, #1, #2** Each counter is identical, and each consists of a 16-bit, pre-settable, down counter. Each is fully independent and can be easily read by the CPU. When the counter is read, the data within the counter will not be disturbed. This allows the system or your own program to monitor the counter's value at any time, without disrupting the overall function of the 8253.

**Control Word Register** This internal register is used to write information to, prior to using the device. This register is addressed when A0 and A1 inputs are logical 1's. The data in the register controls the operation mode and the selection of either binary or BCD ( binary coded decimal )

counting format. The register can only be written to. You can't read information from the register.

**Control Word Register**

| CONTROL BYTE D7 - D0 | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCP |

All of the operating modes for the counters are selected by writing bytes to the control register. This is the control word format.

| D7<br>SC1 | D6<br>SC0 | Counter Select |
|---|---|---|
| 0 | 0 | counter 0 |
| 0 | 1 | counter 1 |
| 1 | 0 | counter 2 |
| 1 | 1 | illegal value |

| D5<br>RL1 | D4<br>RL0 | R / L Definition |
|---|---|---|

Bits D7 and D6 are labeled SC1 and SC0. These bits select the counter to be programmed, it is necessary to define, using the control bits D7 and D6, which counter is being set up.

| | | |
|---|---|---|
| 0 | 0 | Counter value is latched. This means that the selected counter has its contents transferred into a temporary latch, which can then be read by the CPU. |
| 0 | 1 | Read / load least-significant byte only. |
| 1 | 0 | Read / load most-significant byte only. |
| 1 | 1 | Read / load least-significant byte first, then most-significant byte. |

Once a counter is set up, it will remain that way until it is changed by another control word.
Bits D5 and D4 ( RL1 / RL0 ) of the control word shown above are defined as the read / load mode for the register that is selected by bits D7 and D6. Bits D5 and D4 define how the particular counter is to have data read from or written to it by the CPU.

These bits are defined as:

The 1st value, $00, is the *counter latch mode*. If this mode is specified, the current counter value is latched into an internal register at the time of the I/O write operation to the control register. When a read of the counter occurs, it is this latched value that is read.

**Caution:** If the latch mode is not used, then it is possible that the data read back

may be in the process of changing while the read is occurring. This could result in invalid data being input by the CPU ( see the timing diagrams to the 8253 by intel's site or go to page "Memory mapped I/O" ). To read the counter value while the counter is still in the process of counting, one must first issue a latch control word, and then issue another control word that indicates the order of the bytes to be read.

An alternative method of obtaining a stable count from the timer is to externally inhibit counting while the register is being read. To this, an external logic to the 8253 controlled by the Z80 to inhibit count during an input read operation is to connect.

Each technique has certain disadvantages. The first, the latching method, may give the CPU a reading that is "old" by several cycles, depending on the speed of the count and which byte of the counter is being read.

The second method, the external inhibiting function, requires additional hardware. In addition, it may change the overall system operation. The counters 1 and 2 of the MZ-700 are not designed with this additional hardware function. :-( but the counter 0. You can use this method for your own purposes even an amplifier is connected to the output pin of this counter.
The input to counter 0 is 1.1088MHz.

The next 3 bits of the control word are D3, D2, and D1. These bits determine the basic mode of operation for the selected counter. The mode descriptions follows:

| **D3** M2 | **D2** M1 | **D1** M0 | **Mode value** |
|---|---|---|---|
| 0 | 0 | 0 | mode 0: interrupt on terminal count |
| 0 | 0 | 1 | mode 1: programmable one-shot |
| x | 1 | 0 | mode 2: rate generator |
| x | 1 | 1 | mode 3: square wave generator |
| 1 | 0 | 0 | mode 4: software triggered strobe |
| 1 | 0 | 1 | mode 5: hardware triggered strobe |

| D0 | **counts down in** |
|---|---|
| 0 | binary |
| 1 | BCD |

The final bit **D0** of the control register determines how the register will count:

The **maximum values** for the count in each count mode are $10^4$ ( 10,000 decimal ) in BCD, and $2^{16}$ ( 65,536 decimal ) in binary.

Source : http://nprcet.org/e%20content/Misc/e-Learning/IT/IV%20Sem/CS%202252-Microprocessors%20and%20Microcontrollers.pdf