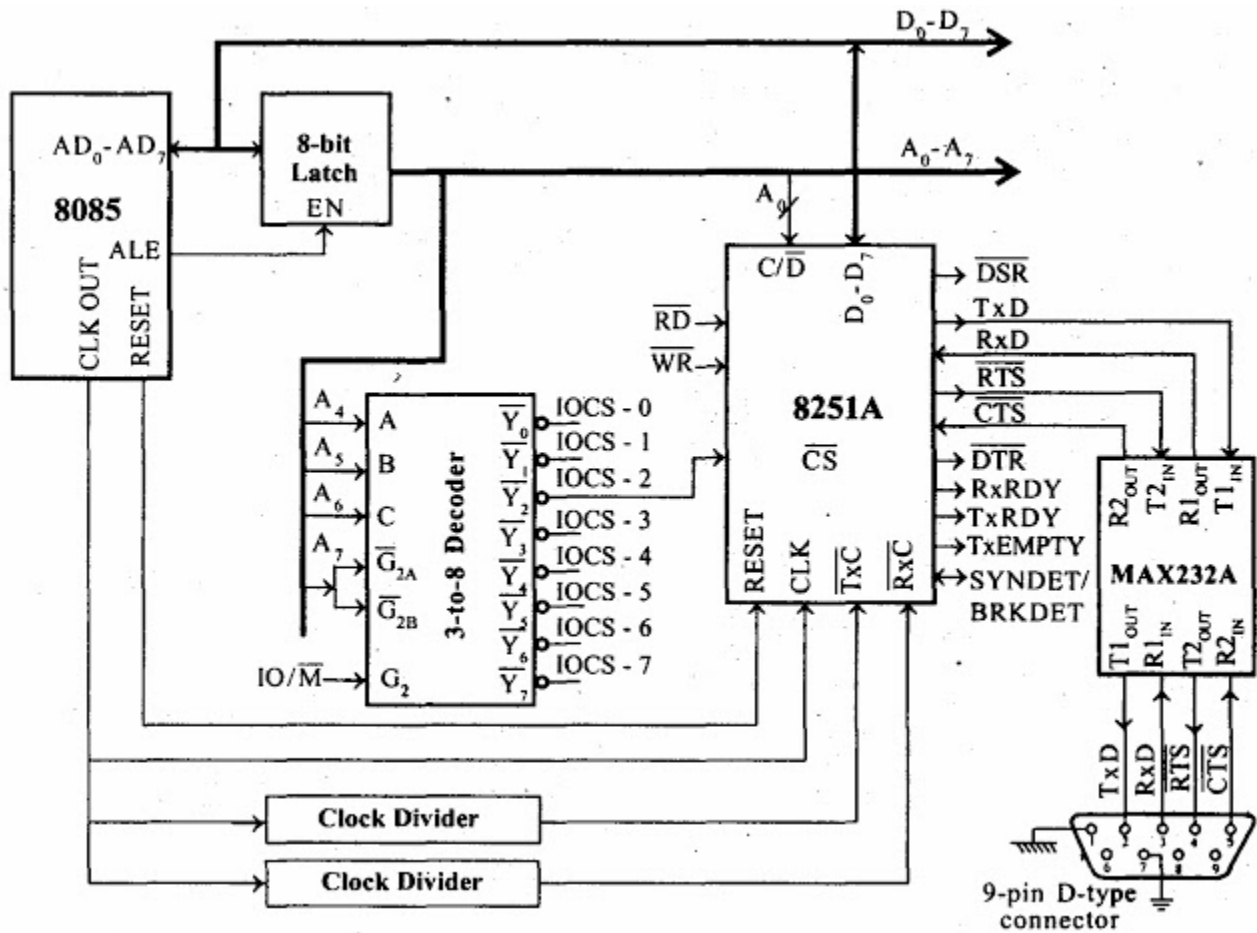


INTERFACING INTEL 8251A WITH 8085 PROCESSOR

The 825 1A can be either memory mapped or I/O mapped in the system.

- 8251A in I/O mapped in the system is shown in the figure.
- Using a 3-to-8 decoder generates the chip select signals for I/O mapped devices.
- The address lines A4, A5 and A6 are decoded to generate eight chip select signals (IOCS-0 to IOCS-7) and in this, the chip select signal IOCS-2 is used to select 8251A.
- The address line A7 and the control signal IO / M(low) are used as enable for decoder.
- The address line A0 of 8085 is connected to C/D(low) of 8251A to provide the internal addresses.
- The data lines D0 – D7 are connected to D0 – D7 of the processor to achieve parallel data transfer.
- The RESET and clock signals are supplied by the processor. Here the processor clock is directly connected to 8251A. This clock controls the parallel data transfer between the processor and 8251A.
- The output clock signal of 8085 is divided by suitable clock dividers like programmable timer 8254 and then used as clock for serial transmission and reception.
- The TTL logic levels of the serial data lines and the control signals necessary for serial transmission and reception are converted to RS232 logic levels using MAX232 and then terminated on a standard 9-pin D-type connector.
- In 8251A the transmission and reception baud rates can be different or same.



- The device which requires serial communication with processor can be connected to this 9-pin D-type connector using 9-core cable.
- The signals TxEMPTY, TxRDY and RxRDY can be used as interrupt signals to initiate interrupt driven data transfer scheme between processor and 8251 A.
- I/O addresses of 8251A interfaced to 8085 is,

Internal Device of 8251A	Binary Address								Hexa Address
	Decoder input and enable				Input to address pin of 8251				
	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
Data buffer	0	0	1	0	x	x	x	0	20
Control register	0	0	1	0	x	x	x	1	21