INTERFACING 8259 WITH 8085 MICROPROCESSOR



• It requires two internal address and they are A =0 or A = 1.

• It can be either memory mapped or I/O mapped in the system. The interfacing of 8259 to 8085 is shown in figure is I/O mapped in the system.

- The low order data bus lines D0-D7 are connected to D0-D7 of 8259.
- The address line A0 of

the 8085 processor is connected to A0 of 8259 to provide the internal address.

• The 8259 require one chip select signal. Using 3-to-8 decoder generates the chip select signal for 8259.

• The address lines A4, A5 and A6 are used as input to decoder.

• The control signal IO/M (low) is used as logic high enables for decoder and the address line A7 is used as logic low enable for decoder.

• The I/O ad4ressès of 8259 are shown in table-8.5.

	Binary Address								
	Decoder input/ enable			Input to address pin of 8259					Hexa address
	Α,	A_6	A,	A ₄	A,	: A,	A ₁	A ₀	
For A_0 of 8259 to be zero	0	0	0	0	x	x	• x	0	00
For A_0 of 8259 to be one	0	0	0	0	x	x	x	1	01

Note : Don't care "x" is considered as zero.

Working of 8259 with 8085 processor:

• First the 8259 should be programmed by sending Initialization Command Word (ICW) and Operational Command Word (OCW). These command words will inform 8259 about the following,

* Type of interrupt signal (Level triggered / Edge triggered).

- * Type of processor (8085/8086).
- * Call address and its interval (4 or 8)
- * Masking of interrupts.

* Priority of interrupts.

* Type of end of interrupts.

• Once 8259 is programmed it is ready for accepting interrupt signal. When it receives an interrupt through any one of the interrupt lines IRO-IR7 it checks for its priority and also checks whether it is masked or not.

• If the previous interrupt is completed and if the current request has highest priority and unmasked, then it is serviced.

- For servicing this interrupt the 8259 will send INT signal to INTR pin of 8085.
- In response it expects an acknowledge INTA (low) from the processor.
- When the processor accepts the interrupt, it sends three INTA (low) one by one.

• In response to first, second and third INTA (low) signals, the 8259 will supply CALL opcode, low byte of call address and high byte of call address respectively. Once the processor receives the call opcode and its address, it saves the content of program counter (PC) in stack and load the CALL address in PC and start executing the interrupt service routine stored in this call address.

Source : http://mediatoget.blogspot.in/2013/02/interfacing-8259with-8085.html