INTERFACING 8251A TO 8086 PROCESSOR

- The chip select for I/O mapped devices are generated by using a 3-to-8 decoder.

- The address lines A5, A6 and A7 are decoded to generate eight chip select signals (IOCS-0
to IOCS-7) and in this, the chip select signal IOCS-2 is used to select 825lA.

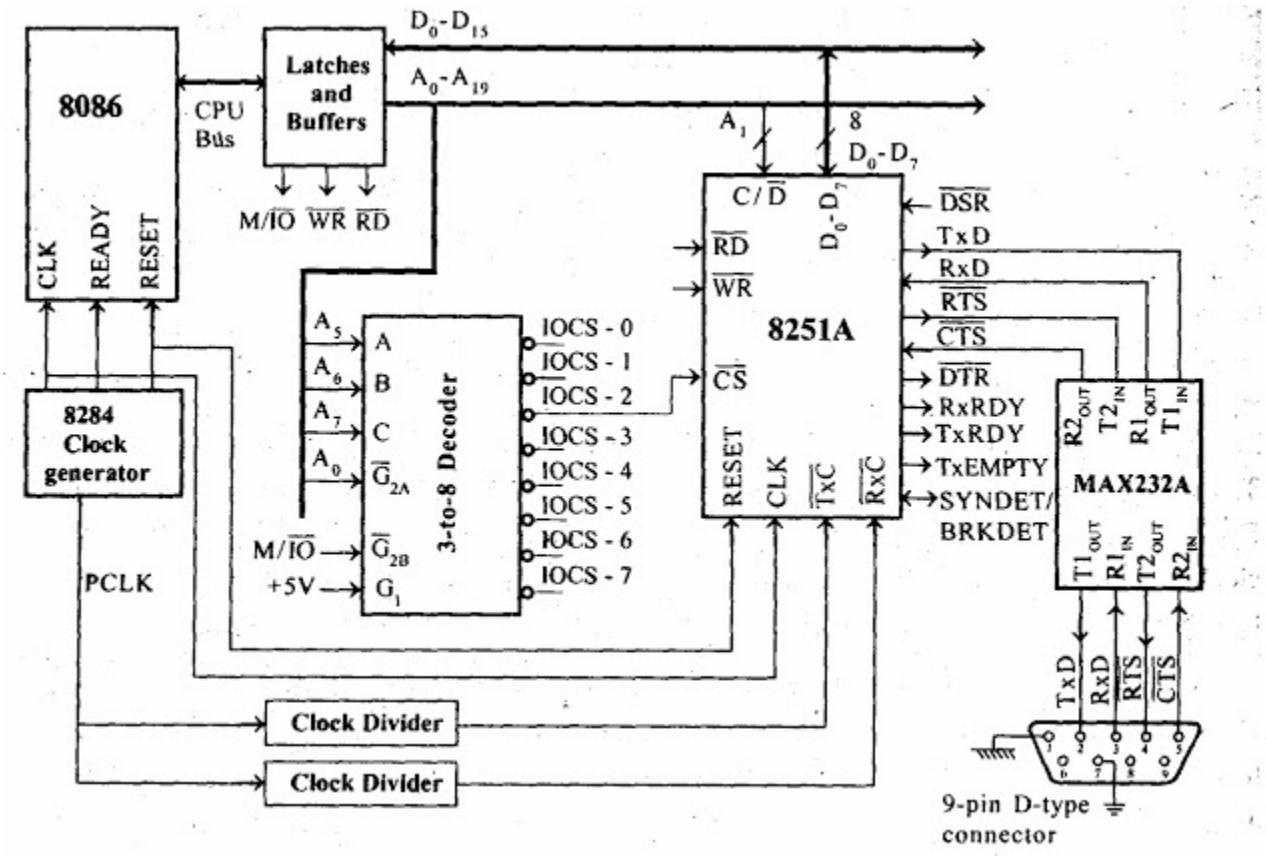
- The address line A0 and the control signal M/IO(low) are used as enable for decoder.

- The line A1 of 8086 is connected to C/D(low) of 8251A to provide the internal addresses.

- The lines D0 – D7 connected to D0 – D7 of the processor to achieve parallel data transfer.

- The RESET and clock signals are supplied by 8284 clock generator. Here the processor
clock is directly connected to 8251A. This clock controls the parallel data transf er
between the processor and 825lA.

- 8251A in I/O mapped in the system is shown in the figure.



- The peripheral clock (PCLK) supplied by 8284, is divided by suitable clock dividers like programmable timer 8254 and then used as clock for serial transmission and reception.

- In 8251A the transmission and reception baud rates can be different or same.

- The TTL logic levels of the serial data lines and the control signals necessary for serial transmission and reception are converted to RS232 logic levels using MAX232 and then
terminated on a standard 9-pin D-.type connector.

- The device, which requires serial communication with processor, can be connected to this
9-pin D-type connector using 9-core cable.

- The signals TxEMPTY, TxRDY and RxRDY can be used as interrupt signals to initiate interrupt driven data transfer scheme between processor and 8251 A.

- The I/O addresses allotted to the internal devices of 8251A are listed in table.

Internal Device of 8251A	Binary Address								Hexa Address
	Decoder input			Input to address pin of 8251				Decoder enable	
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Data buffer	0	1	0	x	x	x	0	0	40
Control register	0	1	0	x	x	x	1	0	42

Source : http://mediatoget.blogspot.in/2013/01/interfacing-8251a-to-8086-processor.html