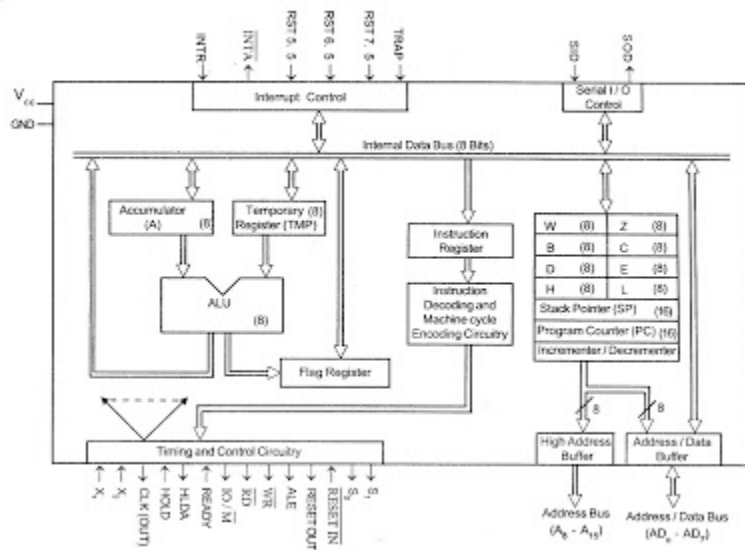


# INTEL 8085 ARCHITECTURE

The architecture of 8085 is shown in figure given below. The internal architecture of 8085 includes the ALU, timing and control unit, instruction register and decoder, register array, interrupt control and serial I/O control.



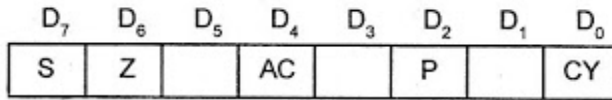
## OPERATIONS PERFORMED BY 8085

The ALU performs the arithmetic and logical operations.

The operations performed by ALU of 8085 are addition, subtraction, increment, decrement, logical AND, OR, EXCLUSIVE-OR, compare, complement and left / right shift. The accumulator and temporary register are used to hold the data during an arithmetic / logical operation. After an operation the result is stored in the accumulator and the flags are set or reset according to the result of the operation.

## FLAG REGISTER:

There are five flags in 8085, which are sign flag (S), zero flag (Z), auxiliary carry flag (AC), parity flag (P) and carry flag (CY). The bit positions reserved for these flags in the flag register are shown in figure below.



**Fig 1.7** : Bit positions of various flags in the flag register of 8085

After an ALU operation, if the most significant bit of the result is 1, then sign flag is set. The zero flag is set, if the ALU operation results in zero and it is reset if the result is non-zero. In an arithmetic operation, when a carry is generated by the lower nibble, the auxiliary carry flag is set. After an arithmetic or logical operation, if the result has an even number of 1 's the parity flag is set, other wise it is reset.

If an arithmetic operation results in a carry, the carry flag is set other wise it is reset. Among the five flags, the AC flag is used internally for BCD arithmetic and other four flags can be used by the programmer to check the conditions of the result of an operation.

#### TIMING & CONTROL UNIT:

The timing and control unit synchronizes all the microprocessor operations with the clock and generates the control signals necessary for communication between the microprocessor and peripherals.

#### INSTRUCTION REGISTER & DECODER:

When an instruction is fetched from memory it is placed in instruction register. Then it is decoded and encoded into various machine cycles.

#### REGISTER ARRAY:

- Apart from Accumulator (A-register), there are six general-purpose programmable registers B, C, D, E, H and L.
- They can be used as 8-bit registers or paired to store 16-bit data. The allowed pairs are B-C, D-E and H-L.
- The temporary registers W and Z are intended for internal use of the processor and it cannot be used by the programmer.
- STACK POINTER (SP):

The stack pointer SP, holds the address of the stack top. The stack is a sequence of RAM memory locations defined by the programmer. The stack is used to save the content of registers during the execution of a program.

- PROGRAM COUNTER (PC):

The program counter (PC) keeps track of program execution. To execute a program the starting address of the program is loaded in program counter. The PC sends out an address to fetch a byte of instruction from memory and increment its content automatically. Hence, when a byte of instruction is fetched, the PC holds the address of the next byte of the instruction or next instruction

#### INSTRUCTION EXECUTION AND DATA FLOW in 8085

The program instructions are stored in memory, which is an external device. To execute a program in 8085, the starting address of the program should be loaded in program counter. The 8085 outputs the content of program counter in address bus and asserts read control signal low. Also, the program counter is incremented.

The address and the read control signal enable the memory to output the content of memory location on the data bus. Now the content of data bus is the opcode of an instruction. The read control signal is made high by timing and control unit after a specified time. At the rising edge of read control signals, the opcode is latched into microprocessor internal bus and placed in instruction register.

The instruction-decoding unit, decodes the instructions and provides information to timing and control unit to take further actions.

Source : <http://mediatoget.blogspot.in/2011/12/intel-8085-architecture.html>