

# INTEGRATED CIRCUIT DESIGN FLOW

The process of chip design is very complex and its understating requires many years of study and practical experience. From a digital integrated circuit design perspective, it could be divided into different hierarchies or stages where the problems are examined at several different levels: system design, logic design, circuit design, layout design, fabrication and testing. These steps are not necessarily sequential; interactions are done in practice to get things right.

**System Design:** This stage provides the specifications and main operations of the chip. It examines such issues like chip area, power, functionality, speed, cost and other design factors while setting these specifications. Sometimes, the resources available to the designer could act as a constraint during this stage. For instance, a designer may like to design a chip to work at 1.2V, but available process technology can only support a voltage of 5V. In this situation, the designer has to adjust these specifications to satisfy the available tools. It is always a good habit to understand the process technology available before system design and specifications. Process technology is basically the specific foundry technology rules where the chip would be fabricated. Typical examples are AMI 0.5um, TSMC 0.35um and IBM 0.13um. A design based on one process technology is unique to that process and accordingly should be fabricated in a foundry that supports that process. At the system design level, the main sections of the system are illustrated with block diagrams, with no details on the contents of the blocks. Only the input and output characteristics of the sections are detailed.

**Logic Design:** At this stage, the designer implements the logic networks that would realize the input and output characteristics specified in the previous stage. This is generally made of logic gates with interconnecting wires that are used to realize the design.

**Circuit Design:** Circuit design involves the translation of the various logic networks into electronic circuitries using transistors. These transistors are switching devices whose combinations are used to realize different logic functions. The design is tested using computer aided design (CAD) tools and comparisons are made between the results and the chip specifications. Through these results, the designer could have an idea of the speed, power dissipation, and performance of the final chip. An idea of the size of the chip is also obtained at this stage since the number of transistors would determine the area of the chip. Experienced designers optimize many design variables like transistor sizes, transistor numbers, and circuit

architecture to reduce delay, power consumption, and latency among others. The length and width of the transistors must obey the rules of the process technology.

**Layout Design:** This stage involves the translation of the circuit realized in the previous stage into silicon description through geometrical patterns aided by CAD tools. This translation process follows a process rule that specifies the spacing between transistors, wire, wire contacts, and so on. Violation of these rules results to malfunctioning chips after fabrication. Besides, the designer must ensure that the layout design accurately represents the circuit design and that the design is free of errors. CAD tools enable checks for errors and also incorporate ways of comparing layout and circuit designs provided in form of Layout Versus Schematic (LVS) checks. When errors are reported, the designer has to effect the corrections. A vital fundamental stage in layout design is Extraction, which involves the extraction of the circuit schematic from the layout drawings. The extracted circuit provides information on the circuit elements, wires, parasitic resistance and capacitance (a parasitic device is an unbudgeted device that inserts itself due to interaction between nearby components). With the aid of this extracted file, the electronic behavior of the silicon circuit is simulated and it is always a good habit to compare the results with the system specification since this is one of the final design stages before a chip is sent to the foundry.

**Fabrication:** Upon satisfactory verification of the design, the layout is sent to the foundry where it is fabricated. The process of chip fabrication is very complex. It involves many stages of oxidation, etching, photolithography, etc. Typically, the fabrication process translates the layout into silicon or any other semiconductor material that is used. The result is bonded with pins for external connections to circuit boards.

Fabrication process uses photolithographic masks, which define specific patterns that are transferred to silicon wafers (the initial substrate used to fabricate integrated circuits) through a number of steps based on the process technology. The starting material, the wafer, is oxidized to create insulation layer in the process. It is followed by photolithographic process, which involves deposition of photoresist on the oxidized wafer, exposure to ultra-violet rays to form patterns and etching for removal of materials not covered by photoresist. Ion implantation of the p+ or n+ source/drain region and metallization to form contacts follow afterwards. The next stage is cutting the individual chip from the die. For external pin connection, bonding is done. It is important to emphasize that this process steps could be altered in any order to achieve specific goals in the design process. In addition, many of these functions are done many times

for very complex chips. Over the years, other methods have emerged. A notable one is the use of insulators (like sapphire) as starting materials instead of semiconductor substrate (the silicon on which active devices are implanted) to build the transistors. This method called Silicon on Insulator (SOI) minimizes parasitic in circuits and enable the realization of high speed and low power dissipation chips.

Testing: The final stage of the chip development is called testing. Electronic equipment like oscilloscopes, probes, pattern generators and logic analyzers are used to measure some parameters of the chip to verify its functionalities based on the stated specifications. It is always a good habit to test for various input patterns for a fairly long time in order to discover possible performance degradation, variability, or failures. Sometimes, fabricated chip test results deviate from simulated results. When that occurs, depending on application, the designer could re-engineer the circuit for improvement and error corrections. The new design should be fabricated and tested at the end.

Source : <http://goafrit.wordpress.com/2009/11/13/integrated-circuit-design-flow/>