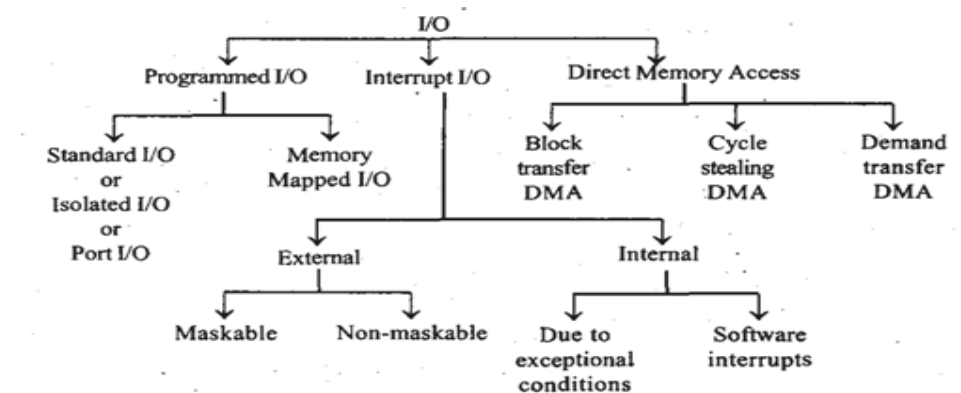


## I/O STRUCTURE OF A TYPICAL MICROCOMPUTER

There are three major types of data transfer between the microcomputer and an I/O device. They are,

- Programmed I/O : In programmed I/O the data transfer is accomplished through an I/O port and controlled by software.
- Interrupt driven I/O : In interrupt driven I/O, the I/O device will interrupt the processor, and initiate data transfer.
- Direct memory access (DMA) : In DMA, the data transfer between memory and I/O can be performed by bypassing the microprocessor.



### INTERFACING I/O AND PERIPHERAL DEVICES:

1. For data transfer from input device to processor the following operations are performed.

- The input device will load the data to the port.
- When the port receives a data, it sends message to the processor to read the data.
- The processor will read the data from the port.
- After a data have been read by the processor the input device will load the next data into the port.

2. For data transfer from processor to output device the following operations are performed.

- The processor will load the data to the port.
- The port will send a message to the output device to read the data.
- The output device will read the data from the port.
- After the data have been read by the output device the processor can load the next data to the port.

- The various INTEL 110 port devices are 8212, 8155/8156, 8255, 8355 and 8755.
- 8212
- The 8212 is a 24 pin IC.
- It consists of eight number of D-type latches.
- It has 8-input lines DI1 to DI8 and 8-output lines DO1 to DO8
- The 8212 can be used as an input or output device
- It has two selecting device DS1 (low) and DS2.

If,

<b>Output Port</b> : When $MD = 1$ , $\overline{DS}_1 = 0$ and $DS_2 = 1$ <b>Input Port</b> : When $MD = 0$ , $\overline{DS}_1 = 0$ and $DS_2 = 1$
---

There are two types for interfacing I/O devices:

1. Memory mapped I/O device.
2. Standard I/O mapped I/O device or isolated I/O mapping.

Memory Mapping of I/O device	I/O Mapping of I/O device
<p>1. 16-bit addresses are provided for I/O devices.</p> <p>2. The devices are accessed by memory read or memory write cycles.</p> <p>3. The I/O ports or peripherals can be treated like memory locations and so all instructions related to memory can be used for data transfer between I/O device and the processor.</p> <p>4. In memory mapped ports the data can be moved from any register to ports and vice-versa.</p> <p>5. When memory mapping is used for I/O devices, the full memory address space cannot be used for addressing memory. Hence memory mapping is useful only for small systems, where the memory requirement is less.</p> <p>6. In memory mapped I/O devices, a large number of I/O ports can be interfaced.</p> <p>7. For accessing the memory mapped devices, the processor executes memory read or write cycle. During this cycle <math>IO/\overline{M}</math> is asserted <b>low</b> (<math>IO/\overline{M} = 0</math>).</p>	<p>1. 8-bit addresses are provided for I/O devices.</p> <p>2. The devices are accessed by I/O read or I/O write cycle. During these cycles the 8-bit address is available on both low order address lines and high order address lines.</p> <p>3. Only IN and OUT instructions can be used for data transfer between I/O device and the processor.</p> <p>4. In I/O mapped ports the data transfer can take place only between the accumulator and ports.</p> <p>5. When I/O mapping is used for I/O devices then the full memory address space can be used for addressing memory. Hence it is suitable for systems which requires large memory capacity.</p> <p>6. In I/O mapping only 256 ports (<math>2^8 = 256</math>) can be interfaced.</p> <p>7. For accessing the I/O mapped devices, the processor executes I/O read or write cycle. During this cycle <math>IO/\overline{M}</math> is asserted <b>high</b> (<math>IO/\overline{M} = 1</math>).</p>

Source : <http://nprcet.org/e%20content/Misc/e-Learning/IT/IV%20Sem/CS%202252-Microprocessors%20and%20Microcontrollers.pdf>