Abstract:

All real systems that work with digitally represented data require error correcting codes because all real channels are noisy to some extent. The basic goal is to control errors in data transmission over unreliable or noisy communication channels. Coding techniques can be divided into two main classes-convolutional and block codes. Convolutional codes are frequently used to correct errors in noisy channels. Viterbi algorithm is a well known algorithm for decoding the received convolutional encoded information sequence to recover original data. Viterbi hard decision decoding algorithm for rate 1/2 and for different generator polynomials is simulated and also implemented on DSP-TMS320C5416.

Keywords: Viterbi, DSP, Trellis, Constraint length.

I. Introduction

The evolving world of telecommunications requires increasing reliability and speed in communications. Reliability in information storage and transmission is provided by coding techniques. Information is usually coded in bit streams and transmitted over the communication medium, channel. The communication media is prone to errors due to noise present in the analog portion of the channel. Therefore errors have to be detected and corrected while decoding. The Error Control Coding techniques (ECC) rely on the systematic addition of redundant bits at the transmitting side. The task of channel coding is to encode information sent over a communication channel in such a way that in the presence of channel noise, errors can be detected and possibly corrected. There are two coding methods - backward error correction codes and forward error correction codes. Backward error correction codes requires only error detection, if an error is found then the transmitter is requested to retransmit the message. Forward error correction codes require the decoder to be capable of correcting errors.

There are several error correcting codes and these are classified under two basic categories namely block codes and convolutional codes. Convolutional codes [1] differ from block codes [2] in the sense that bit streams are not partitioned into binary words instead redundancy is added continuously to the whole stream. Convolutional codes are widely used error control coding technique in channel coding because of low complexity and error controlling capability. Viterbi decoding algorithm [3, 4] is the simplest and best algorithm for decoding of convolutional codes. The Viterbi algorithm first appeared in the coding literature in a paper written by Andrew J. Viterbi in 1967 [5]. Since then, due to its easiness in implementation, it has been applied to many different areas related to decoding problems.

II. Related works

A fuzzy-decision Viterbi decoder is presented in [6] for a Dedicated Short-Range Communications (DSRC) system. The performance of the DSRC system using the proposed fuzzy decision Viterbi decoder is compared with both hard decision and soft-decision Viterbi decoders. The simulation results show that the performance of the proposed fuzzy-decision Viterbi decoder with respect to the hard decision and soft-decision Viterbi decoder is significantly increased. A high performance generic soft input hard output Viterbi decoder is proposed in [7] and prototyped on Field Programmable Gate Array (FPGA) board. The proposed Viterbi decoder is anticipated...
to be used in a complete wireless Local Area Network (LAN) transceiver prototype. The generality of the design facilitates not only the prototyping of Viterbi decoders with different specifications, but also the exploration of the performance of different implementations in order to obtain the most suitable solution for a particular communication system. The Viterbi decoder’s error burst statistics (i.e. burst size and the interarrival times) as a function of signal to noise ratio is analyzed in [8] for two different tactical communications systems, Asynchronous Transfer Mode (ATM) switching system and Internet Protocol (IP) based system which concluded that performance can be improved by including an interleaver to disperse the Viterbi error bursts.

Viterbi decoding has been shown [9] to be a practical method for improving satellite and space communication efficiency by 4 to 6 dB, at a bit error rate of $10^{-5}$. A modified Adaptive Viterbi algorithm, referred to as the relaxed adaptive Viterbi algorithm is presented in [10], which completely eliminates the global best survivor path metric search operation and hence is much more suitable for state-parallel decoder implementation. State-parallel relaxed adaptive Viterbi decoders, can achieve significant power savings and modest silicon area reduction, while maintaining almost the same decoding performance and very high throughput. A reduced state Viterbi algorithm for blind sequence identification of Differentially encoded Phase Shift Keying (DPSK) sources is presented in [11]. It can reduce the number of state in the trellis and hence reduce the computational complexity of Viterbi algorithm significantly while obtaining the full performance benefits. A reconfigurable Viterbi Decoder architecture for Eurecom Mobile platform is presented in [12]. The proposed decoder can be reconfigured online for wireless standards 3GPP, GSM and WLAN 802.11a. A simple Differential Binary Phase Shift Keying (DBPSK) demodulator with 1-bit quantization for both analog and digital part is introduced in [13]. The results show that a DBPSK system with hard-limited digital input benefits from a maximum-likelihood decoding approach when a quadrature demodulator is used. Viterbi decoder for Very Large Scale Integration (VLSI) implementation [14] concludes that power consumption of the Viterbi decoder is significantly reduced when implemented as Complementary Metal Oxide Semiconductor (CMOS) devices.

This paper is organized as follows. Section III gives the proposed work. Section IV explains the simulation model. The results of the proposed model are discussed in section V. Next section concludes the paper.

### III. Proposed Work

The model described in Fig.1 is a simple convolutional encoder and Viterbi decoder. The encoder described in this system is of rate 1/2, and of constraint length -3. Programming is done in ‘C’ language for both coding and decoding and the same is implemented on DSP-5416 kit. Input to encoder is entered by the user. The output of the encoder is stored in the matrix form, and the same is fed to the decoder part.

![Fig.1. Block diagram of the encoder and the decoder](image)

For the implementation of Viterbi decoder algorithm, there are two techniques available: the soft decision decoding and hard decision decoding method. In case of hard decision, the decoder makes a firm or hard decision as to whether one or zero is transmitted and provides no other information regarding how reliable the decision is, hence, its output is only either zero or one (the output is quantized only to two levels) which are called hard-bits. The soft decoder provides the system with some side information together with the decision. The side information provides the decoder with a measure of confidence for the decision. The decoder outputs, which are called soft-bits, are quantized to more than two levels. In this paper the simulation and implementation of Viterbi decoder algorithm is discussed for hard decision decoding method.

Two algorithms are used for the implementation of convolutional coding and decoding, one for the encoder and other for the decoder. Encoder does the work of obtaining convolutional encoded bits for given message bits whereas decoder does the reverse process of it. These two algorithms are as given below.
A. Encoder part:

1. Read the generator polynomial bits.
2. Read number of message bits to be generated.
3. Initialize the state to zero, considering first message bit compute the code by XOR operation. And store the result in a matrix form.
4. Right shift the bits to obtain next state.
5. Repeat steps 3 and 4 for all message bits.
6. Store all the encoded bits and transmit them.

B. Decoder part:

1. Read the received message bits and store them.
2. Give these bits as input to the Viterbi decoder.
3. Compute the accumulated error matrix for received message bits with the help of output table.
4. Select the state having the smallest accumulated error metric and save it.
5. Repeat step 4 until the beginning of the trellis is reached.
6. Decode the message bits.

IV. Simulation Model

The model considered for simulation uses simple encoder and decoder blocks. Simulation is done using ‘C’ and implemented on 5416-Digital Signal Processing kit (version 3.1). The TMS320C5416 DSP Starter Kit (DSK) is a low-cost development platform designed to speed the development of power-efficient applications based on Texas Instruments TMS320C54x DSPs. The C5416 DSK offers the ability to detect, diagnose and correct DSK communications issues, download and step through code faster and get a higher throughput with Real Time Data Exchange (RTDX). It operates at 16 to 160MHz frequency and at ‘+5’V universal power supply. With 160 million instructions per second (MIPS) performance, it can be used as the foundation device for a range of signal processing applications, including speech compression/decompression, speech recognition, text-to-speech conversion, fax/data conversion and echo cancellation.

The TMS320C5416 processor and comprehensive Code Composer Studio development platform can be easily used for software designing. Code Composer Studio features for the TMS320C5416 DSK include a complete Integrated Development Environment (IDE), an efficient optimizing C/C++ compiler assembler, linker, debugger, and an advanced editor with Code Mastro technology for faster code creation, data visualization, a profiler, a flexible manager and a power on self test DSK diagnostic tool as shown in Fig.2 and diagnostic utility to ensure DSK is operating correctly.

![Fig.2. DSK Diagnostic tool](image)

The input to and output from the system are bit streams. The bits entered by the user are used as message/input bit stream to convolutional encoder. A \((n, k, m)\) convolutional encoder accepts \(k\)-bit blocks of input sequence and produces \(n\)-bit blocks of output sequence. It consists of ‘\(m\)’ \(k\)-stage shift registers and ‘\(n\)’ modulo-2 adders. The outputs of ‘\(n\)’ modulo-2 adders are sequentially sampled to produce the encoded sequence. A \((2, 1, 2)\) convolutional encoder is considered for simulation and implementation.
The output of encoder block is given as input to the decoding block. While decoding the proposed code generates output table and next state table depending on generator polynomial and stores them. Basically, decoding of convolutional codes is comparison of different paths in trellis. The trellis diagram for (2, 1, 2) convolutional encoder for generator polynomial \( g_1 = \{1 \ 1 \ 1\} \) and \( g_2 = \{1 \ 0 \ 1\} \) is as shown in Fig.3.

In hard decision decoding technique, the Hamming distance is computed by simply counting how many bits are different between the received encoded bits and the actual output bits. The Hamming distance values are computed at each time instant for the paths between the states at the previous time instant and the states at the current time instant are called ‘branch metrics’. For the first time instant these results are saved as “Accumulated Error Metric” values, associated with the states. For the second time instant on, the accumulated error metrics will be computed by adding the previous accumulated error metrics to the current branch metrics. When two paths enter the same state, the one having the best metric (i.e. lower branch metric) is chosen, this path is called the ‘surviving path’. Then by seeing the path and using output table and next state table decoding is done. This procedure is repeated for all encoded bits and at every comparison makes a hard decision as to whether one or zero is transmitted. The output of hard decision decoder is compared with original message bits for verification.

V. Simulation Results

The simulation and implementation of convolutional encoder and Viterbi decoder is carried out for different message bits and different generator polynomials. The processor implementation results for rate ½ convolutional encoder and Viterbi decoder with generator polynomials \( g_1 = \{1 \ 1 \ 1\} \) and \( g_2 = \{1 \ 0 \ 1\} \) and for message bits (1 1 1 0) are as shown in Fig.4 and Fig.5 respectively.
Similarly the results are verified for generator polynomials by giving different message bits as input. The simulation results of Viterbi decoder for generator polynomials \(g_1 = \{1 1 1\}, g_2 = \{1 1 0\}\) and \(g_1 = \{1 1 0\}, g_2 = \{1 0 1\}\) are as shown in Fig.6 and Fig.7 respectively.

Also different generator polynomials are given as input to the encoder block. The simulation and implementation results exactly matched with the theoretical results. The proposed algorithm is working for all message bits and delivering the expected results.

**Conclusion**

Convolutional Encoder and Viterbi decoder for the rate \(\frac{1}{2}\) is simulated for different constraint lengths. From the simulation it is found that the error recovery capability of the Viterbi decoder varies from generator polynomials as well as for different constraint lengths. Convolutional encoder and Viterbi decoder are successfully implemented on DSP-TMS320C5416.

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Authors

Mr. S. V. Viraktamath is with SDMCET, Dharwad, Karnataka, India. He is serving as Assistant Professor (S.G) in the Department of E&CE. He has received a gold medal from VTU Belgaum for securing first rank in M.Tech (DC&N). He is the Life Member of IETE, IE and ISTE. He has served as a reviewer for many International conferences. His research interests include Error control coding, Wireless communication and Networking.

Dr. G. V. Attimarad is with Dayanand Sagar College of Engineering Bangalore, Karnataka, India. He is serving as Professor in the Department of Electronics and Communication Engineering. His research interest includes area of waveguides and wireless communications. He has published many papers in reputed National and International journals. He is the Life Member of IETE, IE and ISTE. He has served as a reviewer for many International conferences.

Ms Jyoti Madiwalappa Kabbur is pursuing B.E degree in Electronics and Communication Engg. from SDMCET Dharwad, Karnataka, India. At present she is studying in third year. Her field of interest is Information theory and coding and Error control coding techniques.