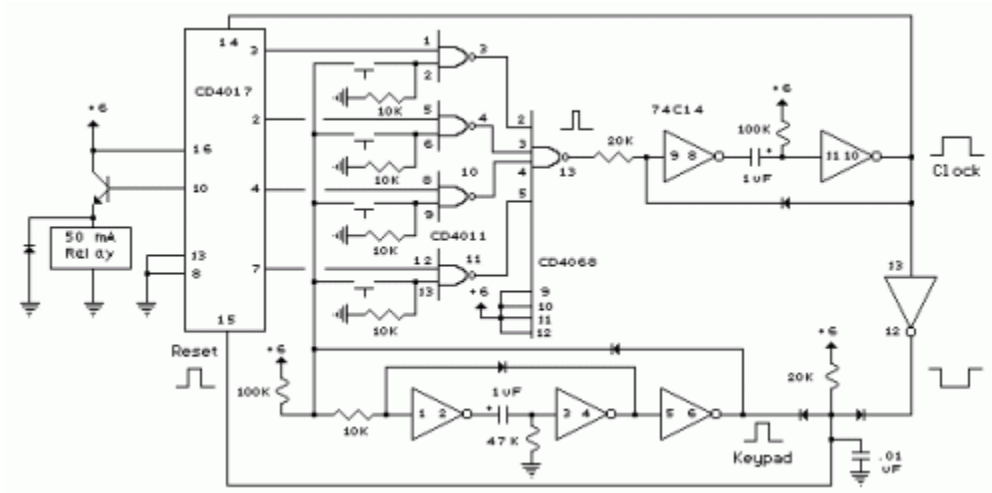


# HOW TO BUILD DIGITAL ELECTRONIC LOCK

## Circuit



## Description

The digital lock shown below uses 4 common logic ICs to allow controlling a relay by entering a 4 digit number on a keypad. The first 4 outputs from the CD4017 decade counter (pins 3,2,4,7) are gated together with 4 digits from a keypad so that as the keys are depressed in the correct order, the counter will advance. As each correct key is pressed, a low level appears at the output of the dual NAND gate producing a high level at the output of the 8 input NAND at pin 13. The momentary high level from pin 13 activates a one shot circuit which applies an approximate 80 millisecond positive going pulse to the clock line (pin 14) of the decade counter which advances it one count on the rising edge.

A second monostable, one shot circuit is used to generate an approximate 40 millisecond positive going pulse which is applied to the common point of the keypad so that the appropriate NAND gate will see two logic high levels when the correct key is pressed (one from the counter and the other from the key). The inverted clock pulse (negative going) at pin 12 of the 74C14 and the positive going keypad pulse at pin 6 are gated together using two diodes as an AND gate (shown in lower right corner). The output at the junction of the diodes will be positive in the event a wrong key is pressed and will reset the counter. When a correct key is pressed, outputs will be present from both monostable circuits (clock and keypad) causing the reset line to remain low and allowing the counter to advance. However, since the keypad pulse begins slightly before the clock, a 0.1uF capacitor is connected to the reset line to delay the reset until the inverted clock arrives. The values are not critical and various other timing schemes could be used but the clock signal should be slightly longer than the keypad pulse so that the clock signal can mask out the keypad and avoid resetting the counter in the event the clock pulse ends before the keypad pulse. The fifth output of the counter is on pin 10, so that after four correct key entries have been made, pin 10 will move to a high level and can be used to activate a relay, illuminate an LED, ect. At this point, the lock can be reset simply by pressing any key. The circuit can be extended with additional gates (one more CD4011) to accept up to a 8 digit code.

The 4017 counting order is 3 2 4 7 10 1 5 6 9 11 so that the first 8 outputs are connected to the NAND gates and pin 9 would be used to drive the relay or light. The 4 additional NAND gate outputs would connect to the 4 remaining inputs of the CD4068 (pins 9,10,11,12). The circuit will operate from 3 to 12 volts on 4000 series CMOS but only 6 volts or less if 74HC parts are used. The circuit draws very little current (about 165 microamps) so it could be powered for several months on 4 AA batteries assuming only intermittent use of the relay.

Source: <http://todayscircuits.blogspot.com/2013/05/how-to-build-digital-electronic-lock.html#.VUCZRNKqpBd>