

# HIGH SPEED SAMPLE AND HOLD CIRCUITS

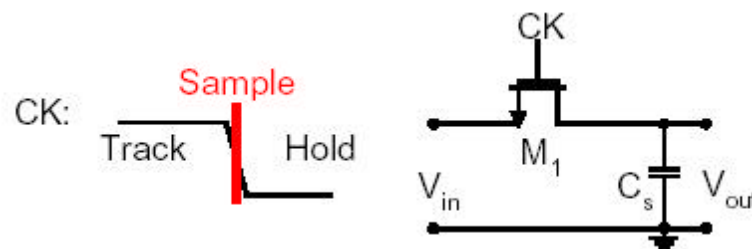
## Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where  $V_{in}$  is the input signal,  $M_1$  is an MOS transistor operating as the sampling switch,  $C_h$  is the hold capacitor,  $ck$  is the clock signal, and  $V_{out}$  is the resulting sample-and-hold output signal.

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As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever



**Figure 1: Simplest sample-and-hold circuit in MOS technology.**

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one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever  $ck$  is high, the MOS switch is on, which in turn allows  $V_{out}$  to track  $V_{in}$ . On the other hand, when  $ck$  is low, the MOS switch is off. During this time,  $C_H$  will keep  $V_{out}$  equal to the value of  $V_{in}$  at the instance when  $ck$  goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

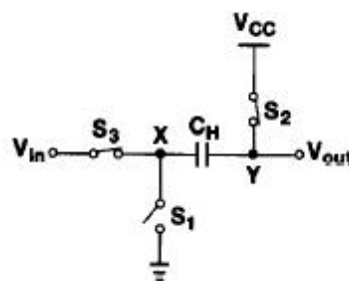
### Alternative CMOS Sample-and-Hold Circuits:

This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.

Series Sampling:

The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled.

On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.



**Figure 2: Series sampling.**

When the circuit is in sample mode, both switches  $S_2$  and  $S_3$  are on, while  $S_1$  is off. Then,  $S_2$  is turned off first, which means  $V_{out}$  is equal to  $V_{CC}$  (or  $V_{DD}$  for most circuits) and the voltage

drop across  $C_h$  will be  $V_{CC} - V_{in}$ . Subsequently,  $S_3$  is turned off and  $S_1$  is turned on simultaneously. By grounding node  $X$ ,  $V_{out}$  is now equal to  $V_{CC} - V_{in}$ , and the drop from  $V_{CC}$  to  $V_{CC} - V_{in}$  is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because  $S_2$  is turned off before  $S_3$ . Thus, the fact that the gate-to-source voltage,  $V_{GS}$ , of  $S_2$  is constant means that charge injection coming from  $S_2$  is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic

capacitance at node  $Y$ . This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that  $C_h$  be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for

series sampling than for parallel sampling. The reason for this is because the value of

$V_{out}$  in series sampling is being reset to  $V_{CC}$  (or  $V_{DD}$ ) for every sample, but this is not the case for parallel sampling.

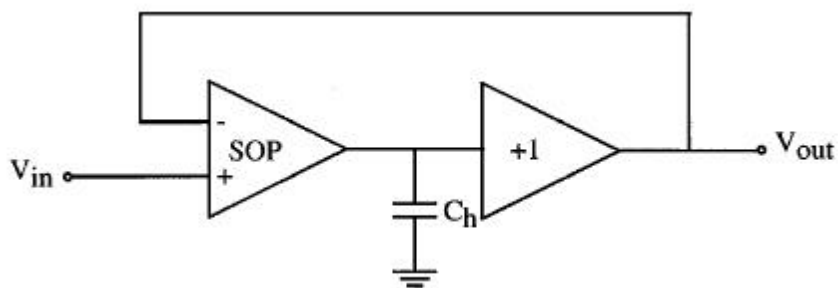
### Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the

saturation region, the channel is pinched off and disconnected from the drain. Therefore,

if the hold capacitor is connected to the drain of the MOS transistor, charge injection will

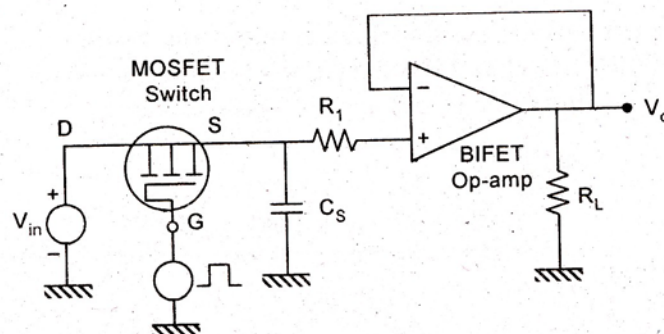
only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 3.



**Figure 3: Switched op-amp based sample and hold circuit.**

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on  $Ch$  to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on  $Ch$  to the output of the S/H circuit.

With the increasing demand for high-resolution and high-speed in data acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed. At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog circuits are now shifted from voltage-mode to current-mode. The advantages of current mode circuits include low-voltage, low-power, and high-speed. Therefore, future researches of S/H circuit should also shift toward current-mode S/H techniques.



The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor  $C_s$  to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Sample-and-hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order to meet the increasing demand for high-speed, low-power, and low voltage S/H circuits for data acquisition systems.

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