High-Density Interconnect

In the 50+ years since printed circuits have become commonplace, the complexity and density of interconnect offered has increased markedly. For example, tracks that were 1mm wide successively became 0.25mm and 150µm, and 100µm is nowadays achievable in volume, although prudence suggests that such densities are not used for large areas. And holes, which used to be 0.9–1.2mm diameter for through-hole connectors, are now typically 0.35mm or less for vias. In other words, conventional printed circuit technology is still capable of meeting many of today's requirements. Yet there is a grouping of products referred to as "High Density Interconnect" (HDI for short) that are used to create still denser interconnect, and it is these that are the subject of this topic paper.

Trend to High Density Interconnect

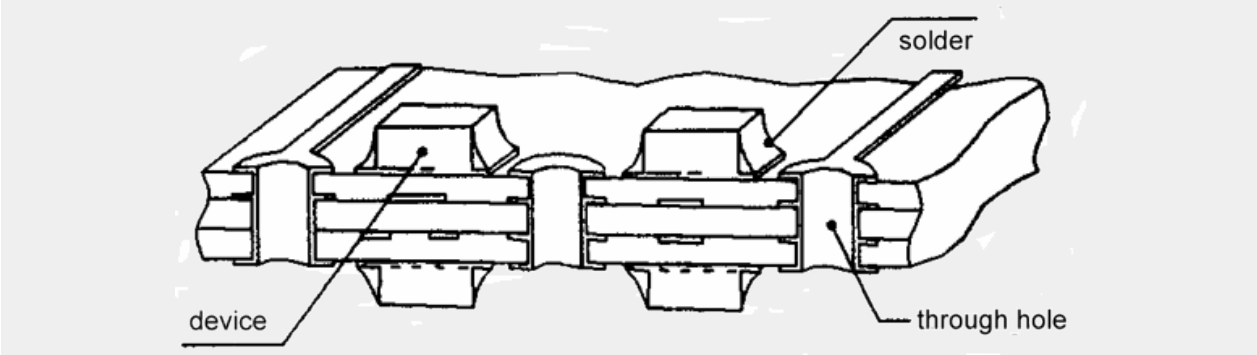
Drivers for higher-density interconnection come under three headings, portability, performance and parts:

- **Portability**, with fast-growing markets for products such as digital cameras, MP3 players and palm computers, all of which represent new opportunities made possible by electronics becoming smaller and lighter.
- **Performance** with increased processing speeds and more RF and microwave communications, at frequencies up to 40GHz in some telecoms areas.
- **Parts**, meeting the silicon challenge to provide more leads in a smaller footprint, which equates to more connections per unit area.

All of these drivers create a demand for denser interconnect, with smaller track and gap dimensions, smaller vias, and more buried vias. Whilst this is not necessarily accompanied by a change in board practice, conventional constructions reach their limits at the bottom end of the size range, so we need to find alternatives.

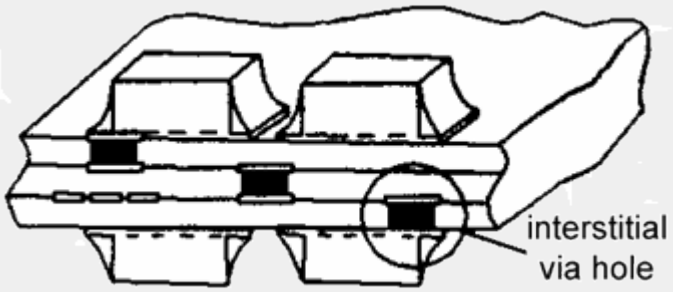
The most significant change between conventional boards and HDI is in the form of the vias. As we show in Figure 1, not only do conventional through vias have sizes that are constrained by the capability of the drilling operation, but they would also normally be kept well away from solder joints in order to avoid solder wicking down the hole. In consequence, conventional assembly designs will employ some separation between components and vias, except where (expensive) buried vias are used.

Figure 1: Component layout with conventional through vias



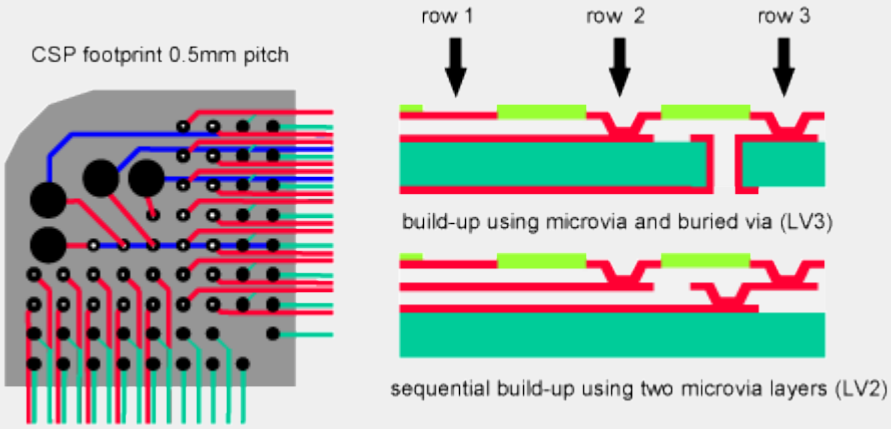
This limitation can be removed by filling the via, either with plated copper or a filled resin, and this increases the available packing density. HDI methods improve the situation further, by making it easier and comparatively cheaper to create vias at arbitrary places within the structure, as indicated in Figure 2.

Figure 2: Component layout using vias within the board structure



This greater freedom is useful both for component placing and the routing of complex components, as this avoids “fan-out” to pads on fine-pitch area arrays, as indicated in Figure 3.

Figure 3: Typical fan-out from a fine-pitch CSP using HDI technology



HDI technology components

There are three main components of High Density Interconnect:

- finer tracks
- smaller (and often filled) vias
- the use of “Sequential Build-Up” technology.

On conventional boards, finer tracks can be made using thinner copper and improved patterning and etching techniques, and it is possible to employ alternatives to drilling to make smaller vias, but what really differentiates HDI from conventional technology is its use of much thinner dielectric layers, building these up either on a “backbone” of

conventional technology, or creating thin composites, such as the Panasonic ALIVH construction we describe later.

We have used the term “microvia”, but without defining it, and a convenient definition is a via whose diameter is 150µm or less, associated with a pad 350µm or less in dimension. Microvias can be “landless”, although they will have a minimal land, and may be blind or buried; they may also be located within pads (“via-in-pad”) or separate.

Definition

Within the context of HDI, blind vias are located in either or both of the outer layers, usually make contact with the first inner layer, and have an aspect ratio of 1:1, as this is compatible with the processes used for their manufacture.

Similarly buried vias, which are between inner layers of the board and do not access the surface layers, are usually between adjacent layers. These restrictions do not apply to conventional boards.

The holes for the microvias may be made by mechanical drilling, but it is more common to use laser ablation, photoimaging, or etching, as will be described later. The via hole may be plated but, equally, filling a microvia with a conductive paste may achieve the same end.

A key to making and filling small holes is to use a very thin layer of dielectric. However, such a thin layer is inevitably very flimsy, so general practice is to build up conductors and dielectric sequentially on a substrate. This substrate itself usually has some interconnection capability, often for power and ground distribution, and a typical board schematic cross-section is shown in Figure 4. Here a four-layer multi-layer conventional board has been built up with successive layers of dielectric and metallisation, with two layers of interconnect on each side, and a final layer carrying the pads.

Figure 4: Schematic cross-section of board stack showing 4-layer core with two build-up layers and one pad-only layer on each side

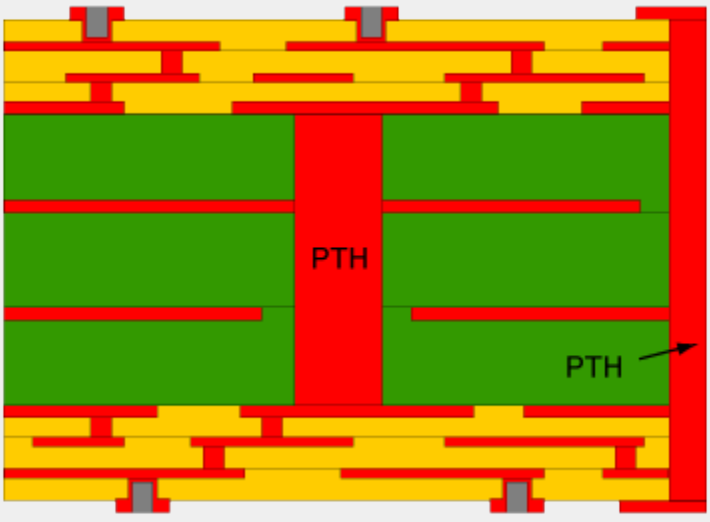
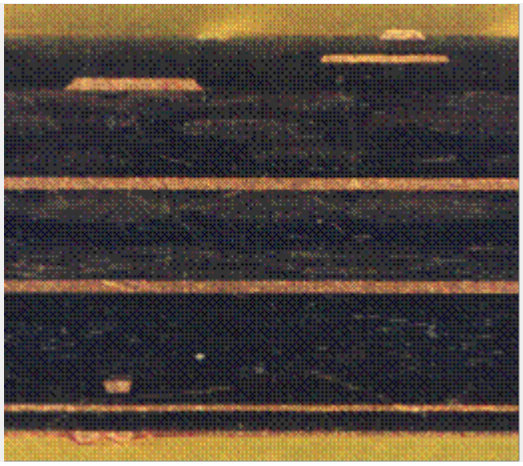


Figure 5 is a cross-section of a real board made using the stack-up shown in Figure 4. Note that the SBU layers are considerably thinner than the conventional dielectric, and

that there is no evidence of reinforcement in the outer layers. This is because glass reinforcement is not compatible with many methods of microvia creation.

Figure 5: Microsection of the board stack shown in Figure 4



Board materials

Having already indicated that there are process compatibility issues when it comes to the choice of SBU materials, it should come as no surprise that there are many other considerations and compromises when it comes to choosing a dielectric material. For example:

- The chemical composition of the dielectric must be compatible with that of the resin in the core substrate
- Material properties such as CTE and glass transition temperature must be sufficiently well-matched between SBU and substrate.
- The SBU dielectric must adhere well to the copper on the core substrate (this can present a challenge).
- From the application point of view, the dielectric properties of the SBU need to be appropriate for the application, bearing in mind the dielectric thickness and trace geometry.
- The construction of the SBU dielectric must allow the reliable formation of microvias, without cracking.
- The SBU dielectric must be able to withstand thermal shocks, for example during soldering.

Clad materials have a long history of use, require fewer process steps, and use the same dielectric and reinforcement as standard PCBs. They can be non-reinforced or reinforced, and are suitable for laser or mechanical via formation.

Unclad materials use additive processes, which are comparatively untested, although they generate less waste. Also, if the materials are not reinforced, vias can be formed by photoimaging. Whilst extra process steps are needed to add copper, this can be an advantage in increased control for high technologies, fine line and controlled impedance.

Although non-reinforced substrates have a lower dielectric constant and may be photoimageable, **reinforced** substrates are generally more stable, have lower CTE and are less sensitive to thermal cracking. However, glass fibres are hard, making them difficult to drill mechanically, particularly when woven, and also reflect/refract laser light. Aramid is an alternative reinforcement that creates laminates which are easier to drill. The generic name is a contraction of “aromatic polyamide”, and a well-known type of aramid fiber (a para-aramid nylon) is commonly known by its trade name, Kevlar™. The equivalent DuPont material used for laminate and prepreg for PCB and semiconductor

Aramid has a low CTE which is a close match to silicon. A best fit between component and substrate CTEs can be achieved using different resin and copper constructions, and this is claimed to enhance reliability by up to ×3. Aramid-reinforced laminates are stable and can be used in very thin layers, but should be employed in combination with a substrate with an aramid-reinforced core.

A common HDI process uses **resin-coated copper foil** (RCF), most often foil with an epoxy-based coating. This is compatible with FR-4 as a core, and is available in different thicknesses to meet dielectric requirements. Two formats are used:

- **one-pass**, with a single B-stage layer to flow and fill
- **two-pass**, with C-stage resin on the foil, and a second coat of B-stage for flow and fill.

The latter provides better thickness control. Alternative resins include PPE for better signal speed.

Platable resins (epoxies; epoxy blends; polyimides) are also used for finer features. These are unclad and non-reinforced, can be laser ablated, and are photoimageable.

By definition, HDI technology is used for fine pitch, complex, densely-packed componentry, so requires a **surface finish** that will give flat, solderable pads. The choices are as with conventional boards, immersion tin or silver competing with ENIG as the main contenders. HASL is generally unsuitable, on account of its surface profile, and OSP is insufficiently solderable after storage.

Microvias

Mechanical drilling is the standard method for creating conventional vias, and suppliers have made real progress in extending the process capability to smaller hole sizes and improved accuracy. However, “best in class” is currently around 100µm diameter, and control of drilled depth (“Z stop”) is difficult, so HDI favours the alternative techniques that are discussed in the following sections.

Laser ablation

There are two methods of laser ablation which can be combined to optimise results:

Photo-thermal ablation uses an *infrared* laser, usually a CO_2 type with wavelength 500–11,000nm, which heats, melts and vaporises material. The laser is pulsed to minimise thermal damage, and 'cuts' dielectric or special clad materials, rather than the copper. The technique has limited capability as diameters reduce.

Photo-chemical ablation uses an *ultraviolet* UV laser, with wavelength below 400nm. High-energy photons break molecular bonds in long-chain organic materials, expanding the material, and ejecting it as powder on the surface. The process is 'cold', so creates no thermal damage, but the laser ablates both dielectric and copper, making good laser control an essential.

There are two distinct categories of UV laser:

UV:YAG , operating at 255–365nm wavelength. This will cut copper and dielectric, and is preferred for holes smaller than 0.5mm diameter. The UV:YAG laser is slow, its speed depends on the diameter, but typically being only 10% that of a CO2 laser. Also, whilst a UV:YAG laser can drill through several layers, good depth control is need to avoid damage Cu layer for via termination

Excimer , operating at 248nm (KrF) or 193nm (ArF) wavelength. this type is comparatively slow (still 10k holes/minute!) and requires an expensive quartz mask.

The three types of laser are compared in Table 1.

Table 1: Comparison of laser methods

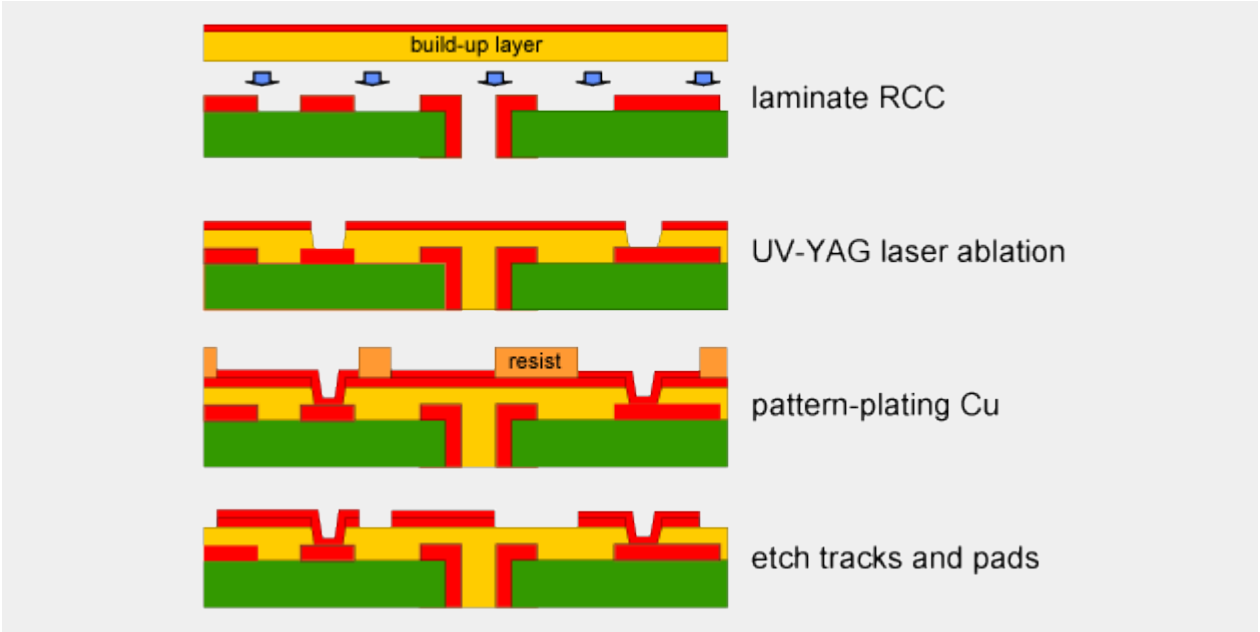
capabilities	excimer	UV:YAG	CO_2
diameter µm	10–100	25–100	70–250
copper	very slow	slow	only for thin oxidised copper
resin (epoxy and polyimide)	slow	slow	fast
FR-4	v. slow	slow	med
hole sharpness	v. good	good	taper
process cost	high	high	low

The process sequence for laser ablation is given in Table 2 and Figure 6.

Table 2: Process sequence for laser ablation

1	Laminate core with RCC or similar material
2a	Use UV laser to ablate copper only (for mixed laser technology, followed by CO_2 laser to ablate resin layer)
or	
2b	Use UV laser to ablate copper and resin
3	Apply conductive ink, and pattern plate and etch as required
4	Repeat to achieve build-up layer circuit requirements

Figure 6: Schematic of sequential build-up using UV-YAG laser technology



Photoimageable dielectric (PID)

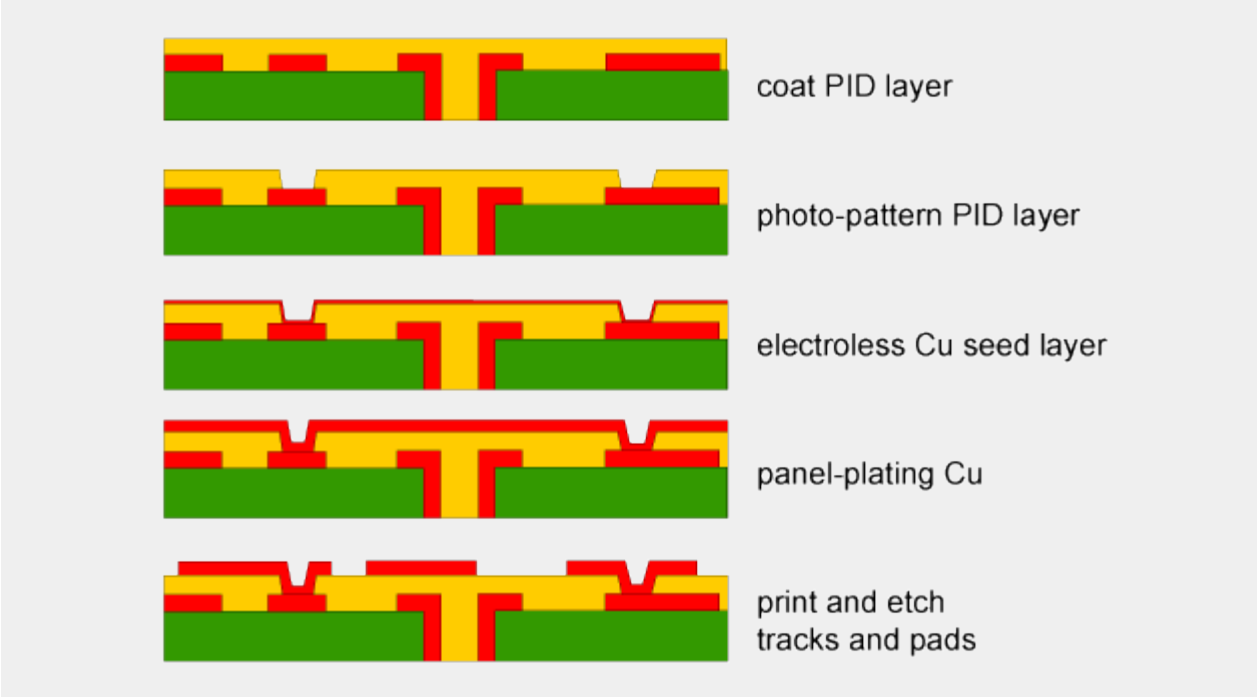
Originally developed in 1990 by IBM Yasu, Japan, photoimaging is an additive (or semi-additive) process capable of creating vias of very small diameter. A mass method, which creates all vias in one layer at the same time, PID is a good process choice for multi-via situations such as area arrays. However, the dielectric thickness is restricted (of the order of 60µm), which may restrict its use for applications requiring high speed or high temperature resistance, and there is a practical problem that dust at the exposure stage can produce unwanted vias.

Photoimaging can be applied to dielectric films that have been laminated or applied by spray, curtain coat, flood screen, or dip, and both positive-working and negative-working chemistries are available. A typical process sequence is given in Table 3 and Figure 7.

Table 3: Process sequence for photoimaging

1	Apply photosensitive polymer to base substrate
2	Expose coating to UV light through a photo-mask tool with the desired circuit pattern, to selectively cross-link the dielectric
3	Develop the dielectric, and remove the material that is not cross-linked, to leave the desired conductor pattern of exposed holes to the copper to which vias are to connect
4	Apply a conductive ink, to fill the exposed holes
5	Apply a second layer of photosensitive dielectric
6	Expose the desired pattern using UV light (as step 2)
7	Develop dielectric and remove uncured dielectric (as step 3)
8	Fill vias with conductive ink as per step 4
9	This can be repeated until the required circuit is formed
10	A final primary resist is applied to complete the outer layer imaging
11	Etch or pattern plate the final circuit

Figure 7: Sequential Build-Up schematic, using photoimageable dielectric process



Plasma etching

Plasma etching has a number of variations, and was popularised by DYconex in their DYCOstrate®, introduced in 1992.

Used for RCC on a base substrate, the plasma used is a mixture of oxygen and carbon tetrafluoride. Two different frequencies of RF excitation of the plasma have been developed:

- microwave – creates high etch rate
- kilohertz – gives uniformity and speed in the Z-axis

Plasma etching has significant limitations, apart from the expense of the special vacuum equipment needed, and is thought to be losing ground to laser ablation and photoimaging:

- limited minimum diameter for vias
- etching is isotropic, leading to under-etching of the metal
- the exposed sharp copper edge can give rise to plating problems
- cannot be used on glass-reinforced materials

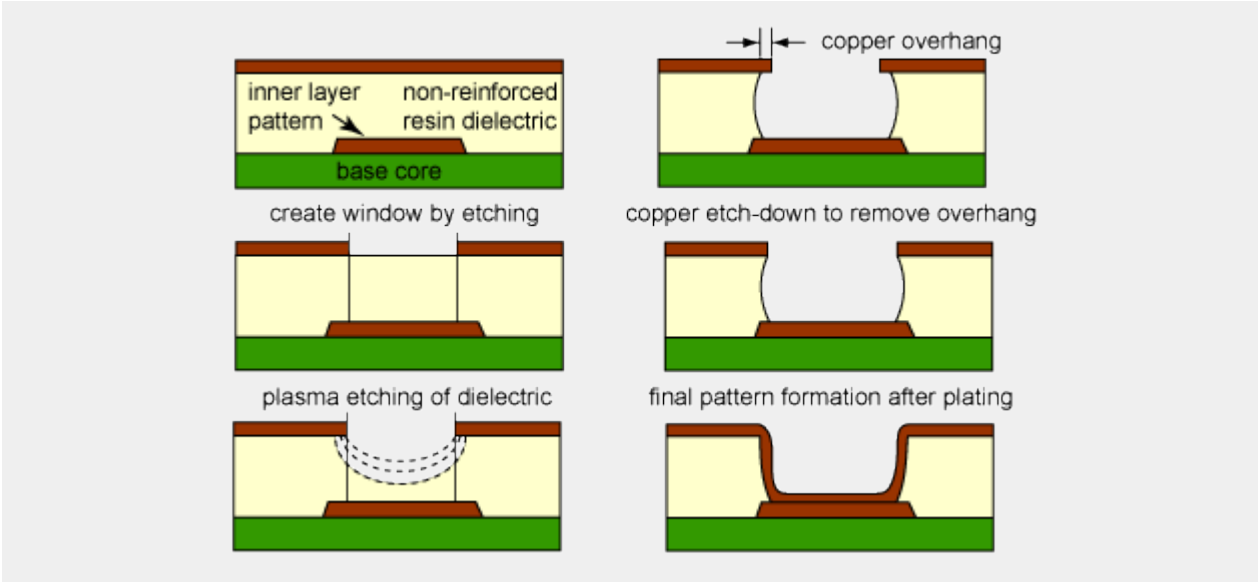
The process sequence for plasma etching is given in Table 4 and Figure 8.

Table 4: Process sequence for plasma etching

1	Fabricate standard PCB core

2	Laminate adhesive RCC to core
3	Print and develop via pattern
4	Etch pattern and strip etch resist
5	Plasma ablate dielectric
6	Etch copper overhang
7	Plate panel with electroless copper
8	Laminate photoresist and develop outer layer image
9	Electroplate
10	Strip resist and etch

Figure 8: The plasma etching process



Wet etching is an alternative method for mass via formation, using the fact that polyimide films will dissolve in hot potassium hydroxide solution. As with plasma, etching is isotropic, leading to undercutting of the copper top surface, which makes subsequent via metallisation more complex.

The methods compared

How these processes compare is described in Tables 5 and 6, from which it will become clear that there are many options and “horses for courses”:

Table 5: Materials compatibility

technology	standard Cu foil	RCC	thermally cured resin	photoimage resin
photo via	no	no	no	yes
CO_2 laser	yes	yes	yes	yes
YAG laser	yes	yes	yes	yes
plasma	no	yes	no	no

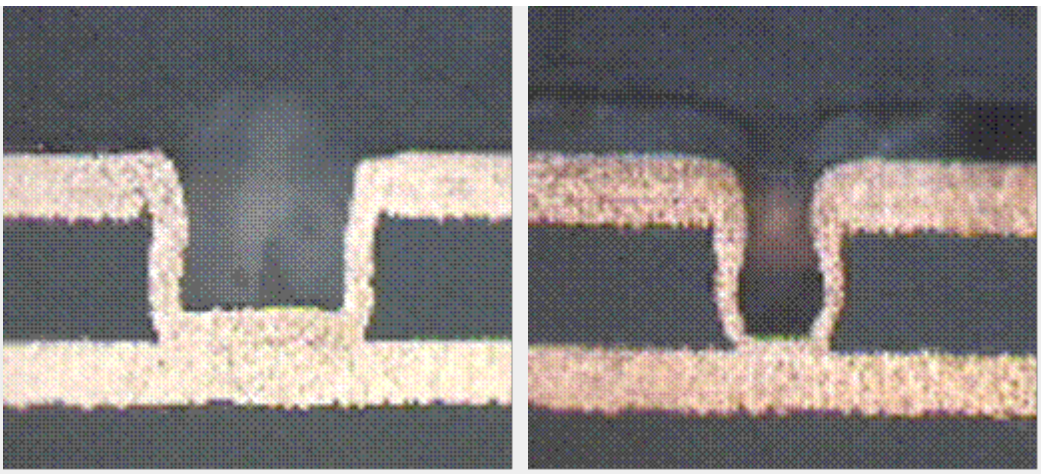
Table 6: Microvia process comparisons

characteristic	photo-liquid	photo-film	laser-RCC	laser-MP	plasma
dielectric cost	medium/high	high	high	medium/high	high
via size (lab)	50µm	100µm	75µm	100µm	100µm
line width	75	75	100	100	75
line space	75	75	100	100	85
via diameter in production	125	125	100	175	100
max via layers	3×2	1×2	1×2	8	4
dielectric thickness	40–80	60–80	60	100–250	50
dielectric thickness control	difficult	good	good	good	good
dielectric constant	3.8	3.8	3.8	3.5	3.5
glass transition temperature	130°C	170°C	170°C	170°C	170–200°C

process issues	pinholes	conformability	conformability	via filling	via shape
process issues	adhesion	adhesion	hole cleaning		non-uniform via
process issues	thickness control				slow process

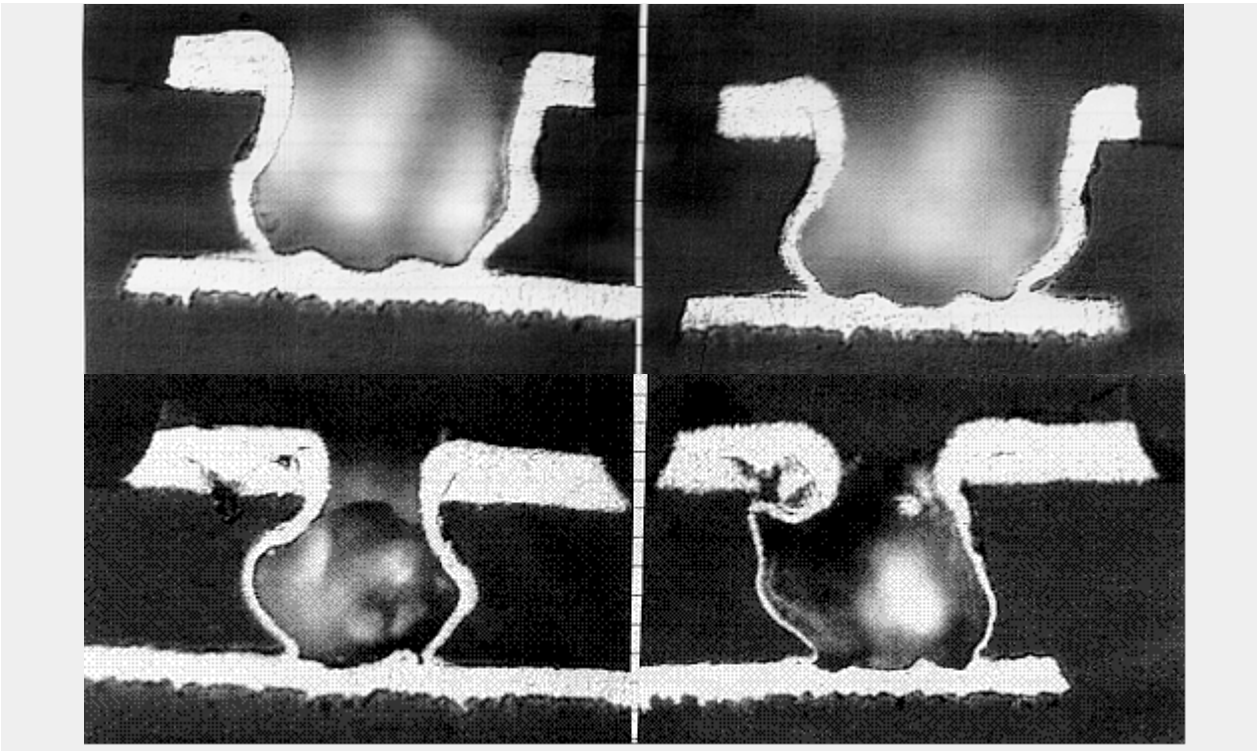
Via quality is important in making a reliable product. One aims for vias that look similar to those shown in Figure 9.

Figure 9: Laser microvias in RCC 125µm diameter (left); 75µm diameter (right)



However, problems can occur with both forming and plating, as shown in Figure 10.

Figure 10: Poorly formed and plated vias 100µm holes, with 5µm plating (left) nominal 75µm holes, actually only 45µm, with 1–2µm plating (right)



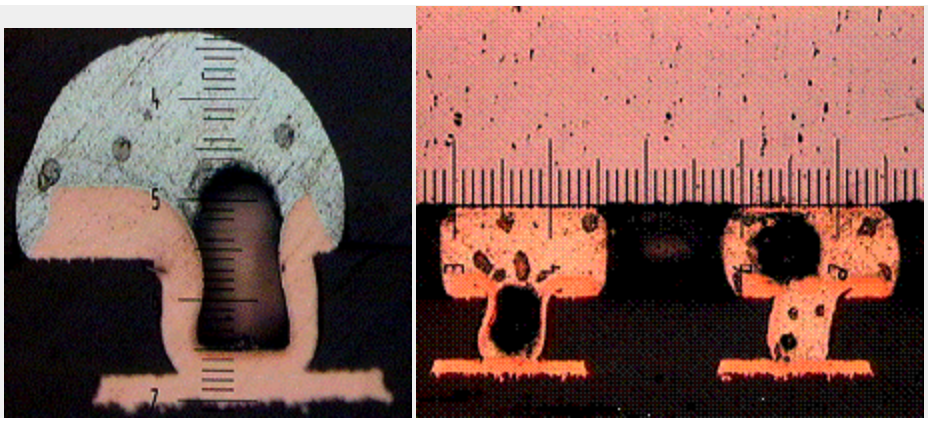
Via filling and plugging

Vias may be left unfilled, but this can create assembly problems

- solder robbing from joint (solder wicks down hole)
- possible chip skewing (solder wicking causes surface tension effects on chip)
- possible tombstoning (uneven heating)
- if through the PCB, can cause QFP/BGA reflow or joint damage

There are also definite disadvantages to having an unfilled via-in-pad. Figure 11a shows a cross-section of a well-formed via, with no component fitted, but solder paste printed and reflowed. Notice the air-pocket trapped in the via. Whilst acceptable the air-pocket is potentially mobile during soldering (Figure 11b), and the resulting voids may constitute a reliability risk

Figure 11: Cross-section of well-formed via, with air-pocket trapped in the via (left) Cross-section of unfilled vias showing variable positions of the resulting voids (right)



There are many potential ways of filling vias:

- plating with copper
- applying a dual-cure (UV + heat) epoxy or acrylic resin by screen printing
- using photoimageable dielectric (sometimes needs two passes)
- applying a conductive paste by printing or doctor-blading
- using solder mask
- using resin-coated foil

Of course, from a fabricator's perspective, filling vias is an extra process (therefore longer lead-time and higher cost) and via-in-pad is correspondingly unpopular as a process variation.

It is also a process that can cause problems if incorrectly carried out. The cracking and incomplete filling shown in Figure 12 left, and bubbles in the plug (not illustrated), can cause flux entrapment and solder balling and also trap harmful contaminants. Conversely, overfilling (Figure 12 right) causes the stencil to be held off the board surface, leaves indents in the stencil, and can even damage metal squeegees.

Figure 12: Via-plugging defects Cracking and incomplete filling (left) Over-filling (right)

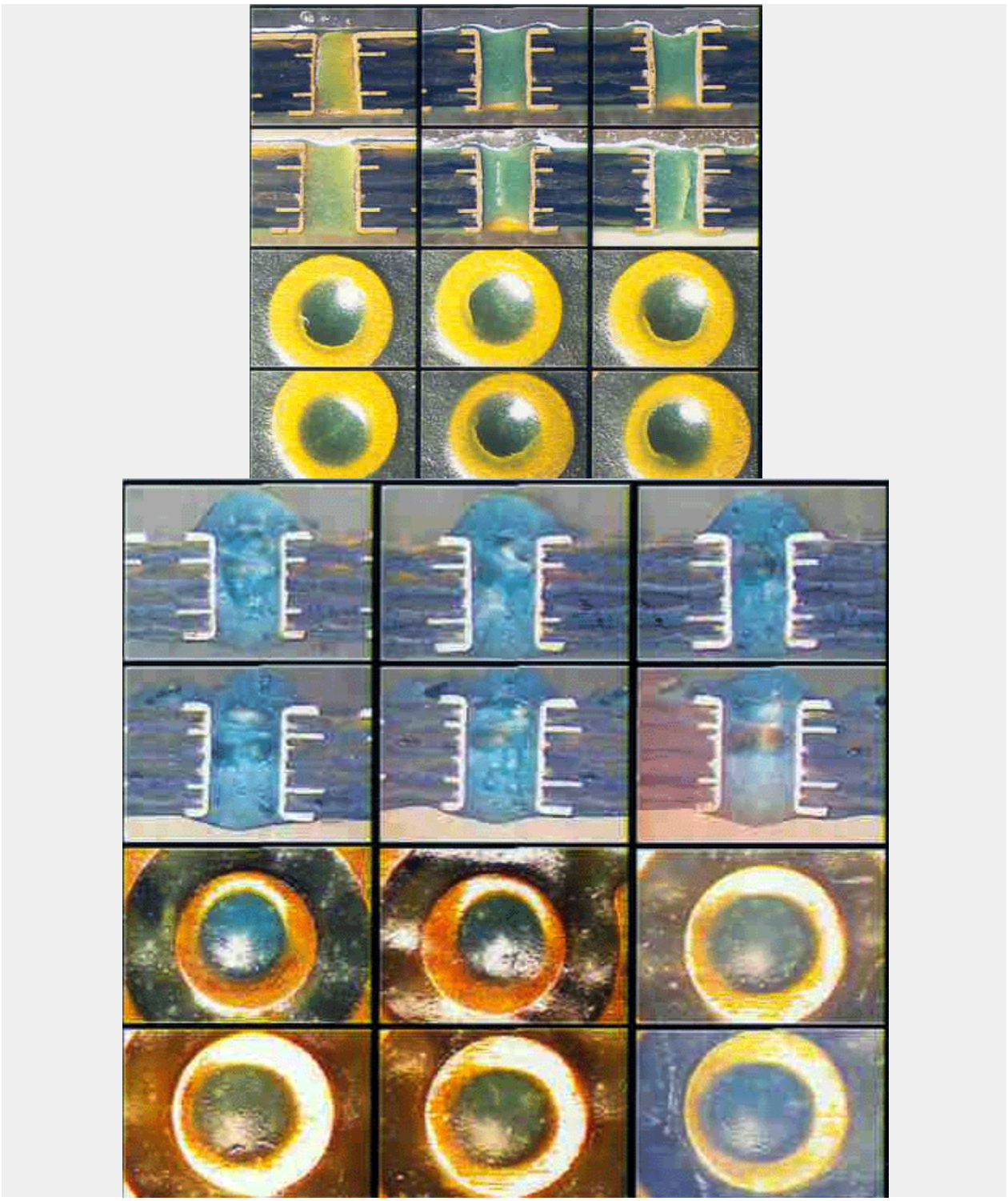
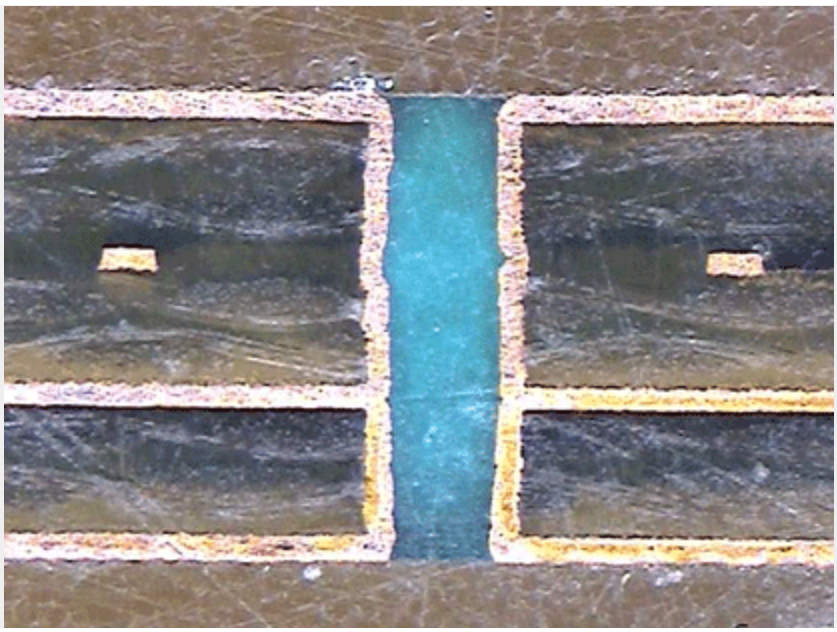


Figure 13 shows the target for a filled via, albeit one that is a conventional via rather than an HDI type.

Figure 13: Well-filled via, flush with surfaces of board



Practical HDI implementations

There are many commercial HDI supplier, each with their own processes. We have already mentioned Dyconex, and encourage you to look for others. In this brief section, we concentrate on two rpocesses that

ALIVH (Any-Layer Interstitial Via Hole) was developed by Matsushita (Panasonic) for use in portable applications such as cell phones and notebooks. A simple process, which uses some conventional PCB techniques, ALIVH has the key advantages that the board is very thin and light, and the time to design and manufacture is very short.

ALIVH (Figure 14) uses a non-woven aramid laminate, with high-speed laser drilling to create 200µm vias that are filled with copper-loaded polymer paste, and with fine-line patterning (60µm track; 90µm gap). The process sequence is shown in Figure 15.

Figure 14: ALIVH construction

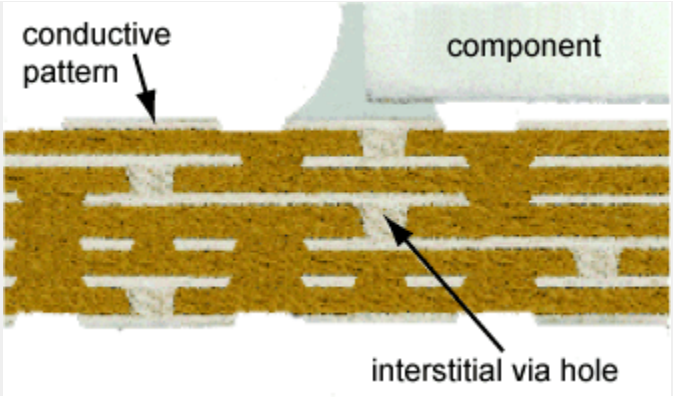
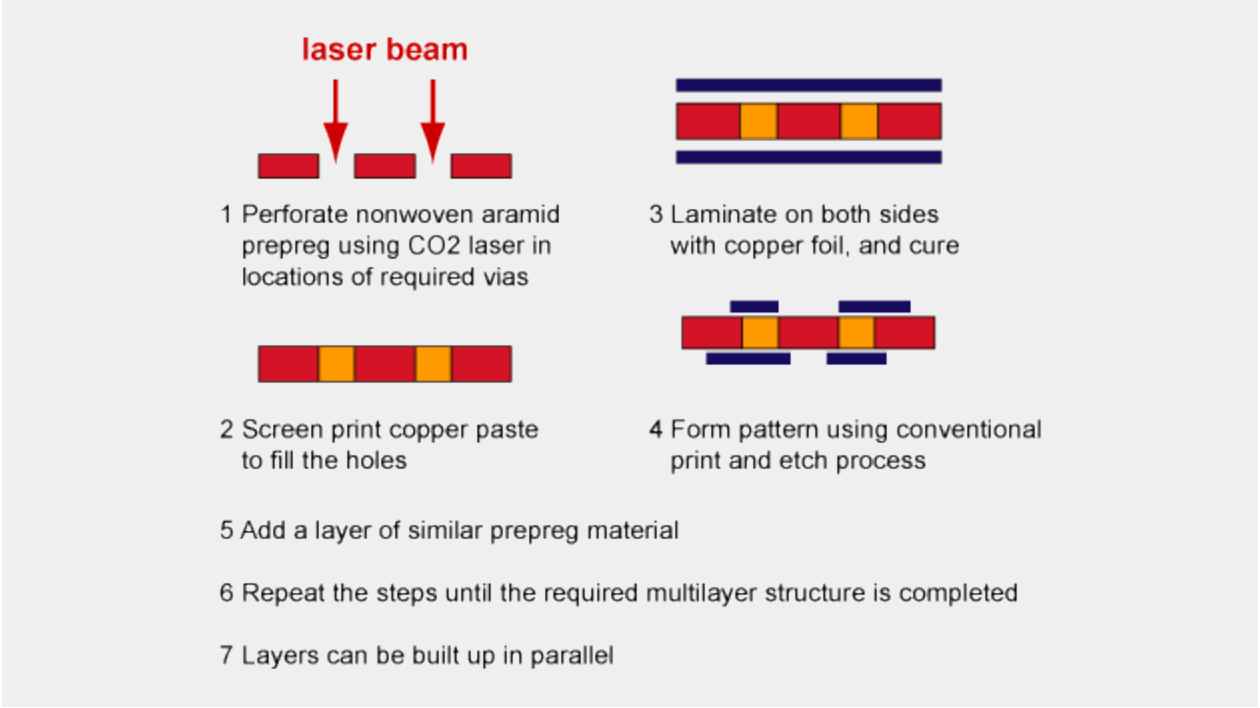


Figure 15: The ALIVH process sequence



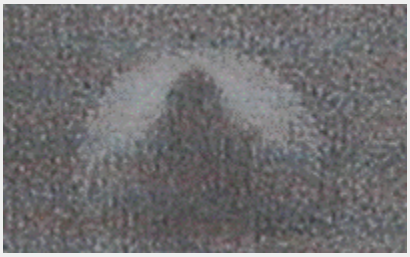
ALIVH allows designers freedom of component placement, including over vias, and in cell phone applications has been shown to reduce overall board size by 30–50%, creating a 6-layer board typically 0.7mm thick (against a 0.9mm conventional board).

Design limitations are in the final board size (200–250mm), in the practical layer count (maximum of 10 due to the sequential nature of the process) and in the hole diameter (limited by the prepreg thickness).

Assembly problems are created by the thinner board, which requires extra care in handling and board support during reflow soldering, and by the tendency of the ALIVH structure to absorb moisture, which requires care with storage and often pre-baking.

Toshiba developed their **B2it** process using silver paste to form a microvia structure. B2it can be used to build up all layers, or can build onto a standard laminate structure. The process sequence is shown in Table 7

Table 7: The B2it process

1	Screen print silver paste onto adhesive side of copper foil of base laminate through metal stencil (may take several passes). Dry the paste.	

2	Take single sided copper on dielectric sheet, and press dielectric onto metal cones of dried paste. The cone pierces through the dielectric, to contact the copper.	
3	Apply thermal compression to complete the structure.	

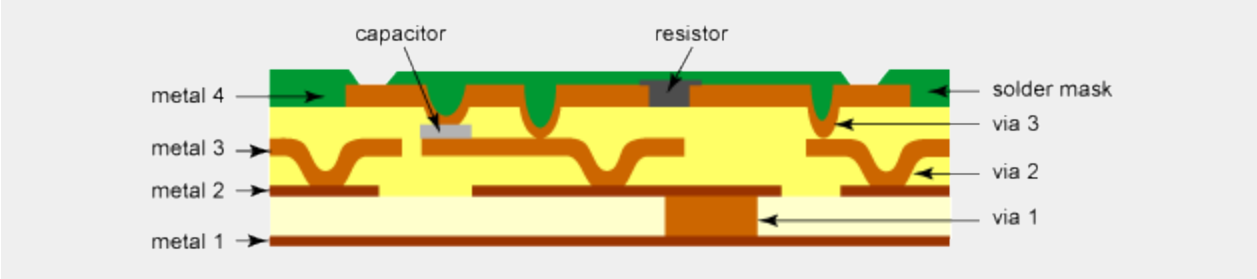
As with all technologies, the boundaries continue to be pushed, as indicated in Table 8.

Table 8: B2it design limitations

design feature	current	future
conductor width/space	100µm:100µm	50µm:50µm
bump diameter	300µm	100µm
pad diameter	500µm	200µm
bump pitch	600µm	300µm

An HDI structure, which is built of a number of thin interleaving layers of metal and dielectric, built up sequentially onto a stable substrate, lends itself to having **components integrated into the structure**. Typically these will only be resistors, made using a polymer thick film material, and capacitors, created by depositing areas of high-dielectric constant material, as indicated in Figure 16. There are limitations on resistor stability and accuracy, although parts can be laser-trimmed to value before solder mask is applied. Similarly, there are limitations as to the value and tolerance of capacitors.

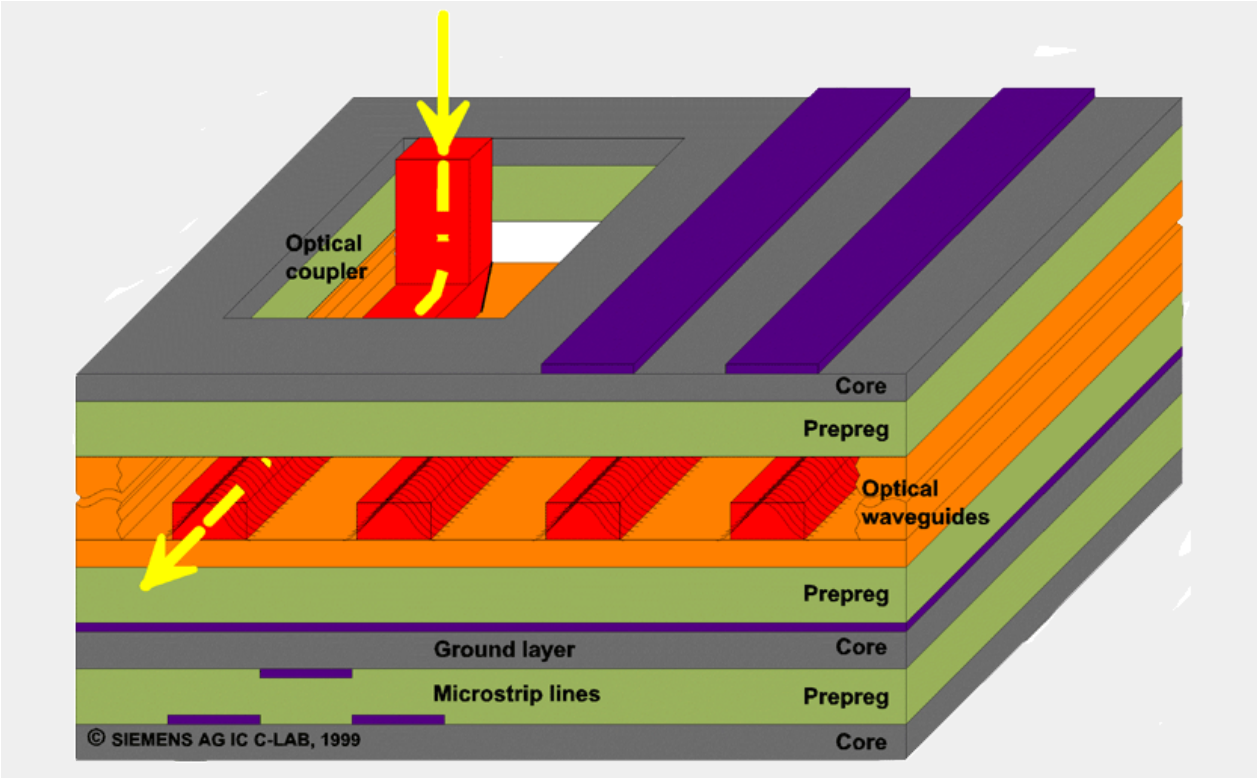
Figure 16: HDI with integral components



Should one embed components? Some thoughts on this in Richard Snogren's *When to embed: advice on factors to consider and questions to ask before layout*, in *Printed Circuit Design and Manufacture*, February 2004.

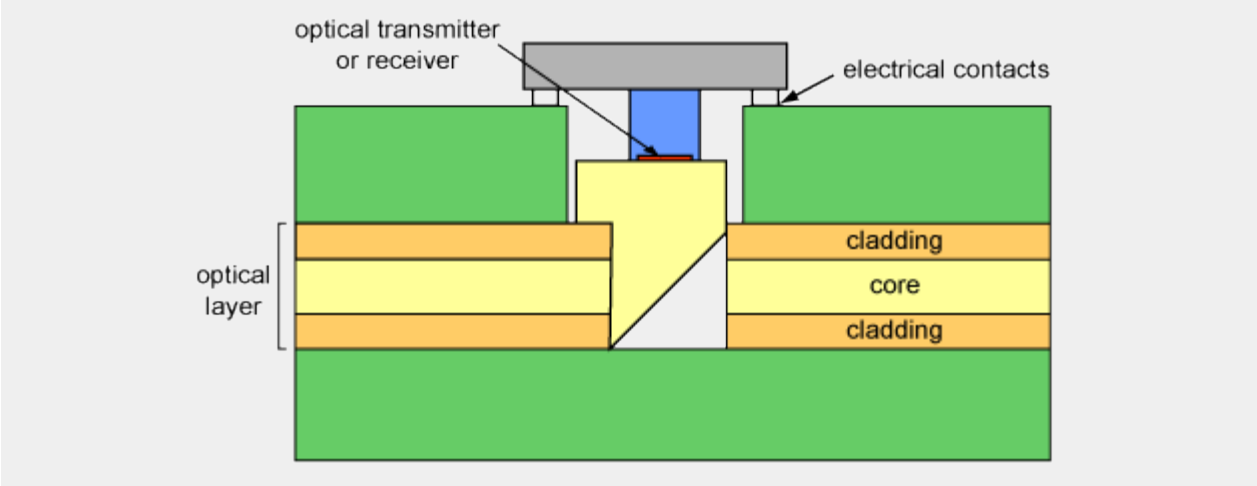
The overall process for making HDI parts involves both conventional lamination and sequential build-up techniques, so is relatively complex. At the same time, having such a composite structure allows other types of elements to be embedded, as with the optical waveguides shown in Figure 17.

Figure 17: Specialist case of HDI, with optical waveguides within substrate structure



Clearly one of the areas of difficulty is creating an appropriate coupling, and an indication of how Siemens approach this is shown in Figure 18.

Figure 18: Coupling to an embedded waveguide



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