Getting Started With FPGAs



So today, I thought I would talk about something other than microcontrollers. Today, I will talk about how to get started with FPGAs.

What is a FPGA?

An FPGA is a field programmable gate array. Instead of programming a FPGA like your standard microcontroller, you actually "implement" digital circuits using a hardware description language (HDL). The two common hardware description languages includes VHDL and Verilog. For today's tutorial, we'll implement our design using Verilog.

FPGA vs Microcontrollers

So what are the advantages of using a FPGA rather than a microcontroller? The problem with microcontrollers is that they cannot run co-currently, or only run sequentially, and very time limited. A FPGA runs in parallel, or able to run multiple things at once, and much faster than microcontrollers. However, FPGAs are very space limited and initially does not come with all of the fancy peripherals that microcontrollers have. Things like timers, UART, and SPI must be implemented by hand on the FPGA. Also, to have your design stay with the FPGA, you have to use a re-programmable flash memory IC.

Parts List

To get started, you need only the following items

Hardware

- Basys 2 Board (100 die)
 Software
- Xilinx Web ISE
- Digilent Adept

Installing Xilinx Web ISE

• To learn how to install the Xilinx Web ISE, I highly recommend visiting this URL .They have all the necessary information on properly installing the ISE.

Installing Digilent Adept

• To program the Basys 2 board, you need to download Adept from Digilent's website. Just follow the on screen prompts for proper installation.

Starting A Project

- To create a new project, go to file->new project
- At the create project screen, select a name and location for the project. For this example, let's name the project "First_Project" and set the location to any location on your computer. Make sure you select "HDL" as your Top-level source type.

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- For project settings, make sure you have the following set...
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- 2. Device is XC3S100E
- 3. Package is CP132
- 4. Speed is ~4
- 5. Synthesis Tool is XST (VHDL/Verilog)
- 6. Simulator is ISim (VHDL/Verilog)
- 7. Preferred Language is Verilog

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• At Project Summary, select Finish.

Creating Verilog Module

 At the project menu, you should see x3s100e-4cp132. Right click on this and select "New Source"

| Select Source Type Select source type, file name and its location. IP (CORE Generator & Architecture Wizard) Schematic User Document Verilog Module Verilog Test Fixture | |
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| VHDL Module VHDL Library VHDL Package VHDL Test Bench Embedded Processor | File name: blink Location: C:\Users' |

- At the new source menu, select Verilog module and set the name to blink.
- When prompted at the define module, just click next. We'll define the inputs and outputs later on. Afterwards select finish.
- In your blink.v file, copy and paste the following code into the file.
- Make sure to hit save.

Creating UCF File

Although we created the module, the FPGA does not know which pins on it should be connected to the module's inputs and outputs. This is where the UCF file comes in.

- Right click you blink.v file and select "New Source"
- In your new source menu, select "Implementation Constraints File." We'll name this file "blink". Don't worry, this will not replace the blink.v file.

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- Hit next and select finish
- In your blink.ucf file, copy and paste the following code.
- Make sure to hit save.

Creating Bit File

Okay, so we're almost ready to program- I mean " implement"- our digital design on the FPGA. FPGAs are usually programmed using a bit file. We're going to create a bit file using the Web ISE.

- Click on blink.v in your project navigator
- Your should see "Generate Programming File" in the Processes menu. Click on it.

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• Wait for a little bit for the ISE to finish creating the bit file.

Checking Connections

It is very important to check to see if the FPGA really routed the inputs and outputs correctly. To do this...

- Click on your blink.v file
- In the Processes menu, select " Design Summary/Reports"
- In Design Overview click on "Pinout Report"
- Check to see if "clk_in" is connected to B8 and "out" is connected to M5.

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• As shown above, the ISE did not correctly route the connections. This can be solved by resaving your UCF file and clicking the "Generate Programming File" option again.

Uploading the Digital Design To The FPGA

We're at the final part of the tutorial!

- Open Digilent Adept
- Connect the Basys 2 to your computer and turn on it on.

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- You can upload the bit file to the main FPGA or the board's re-programmable flash memory. Since we want the board to remember the bit file whenever we turn on or off the board, we'll program the bit file to the reprogrammable flash (PROM)
- Click browse button next to the PROM option
- Navigate to your project folder. The bit file should be inside the folder.
- Hit "program" next to browse
- After the bit file is uploaded to the board, turn off then turn on your board. You should see LD0 blink every 500ms.

How does it work?

First thing, we need to use the 50MHZ clock on the board to tell the FPGA when 500ms has occurred. But how? Well, frequency is really counts per second. Using unit conversion and an onboard counter, we can find how many counts it takes for 500ms to occur.

 $\frac{50,000,000}{seconds} * 500ms = 25,000,000$

Now that we know the counts, how do we use it in our design? We can use a register, a variable inside verilog, to function as our counter. During the positive edge of the clock, we tell the design to increment the counter by 1. When counts reaches 25 million, the design resets the counter to 0 then invert the output of the LED, which is initially set to off.

Source: http://coolcapengineer.wordpress.com/2013/05/06/tutorials-gettingstarted-with-fpgas/