

## GENERAL LAYOUT GUIDELINES

1. The electrical gate design must be completed by checking the following
  - a. Right power and ground supplies
  - b. Noise at the gate input
  - c. Faulty connections and transistors
  - d. Improper ratios
  - c. Incorrect clocking and charge sharing
2. VDD and the VSS lines run at the top and the bottom of the design
3. Vertical polysilicon for each gate input
4. Order polysilicon gate signals for maximal connection between transistors
5. The connectivity requires to place nmos close to VSS and pmos close to VDD
6. Connection to complete the logic must be made using poly, metal and even metal2

The design must always proceed towards optimization. Here optimization is at transistor level rather than gate level. Since the density of transistors is large, we could obtain smaller and faster layout by designing logic blocks of 1000 transistors instead of considering a single at a time and then putting them together. Density improvement can also be made by considering optimization of the other factors in the layout.

The factors are

1. Efficient routing space usage. They can be placed over the cells or even in multiple layers.
2. Source drain connections must be merged better.
3. White (blank) spaces must be minimum
4. The devices must be of optimum sizes.
5. Transparent routing can be provided for cell to cell interconnection, this reduces global wiring problems

## 2.10 LAYOUT OPTIMIZATION FOR PERFORMANCE

1. Vary the size of the transistor according to its position in series. The transistor closest to the output is the smallest. The transistor nearest to the VSS line is the largest. This helps in increasing the performance by 30 %. A three input nand gate with the varying size is shown next.

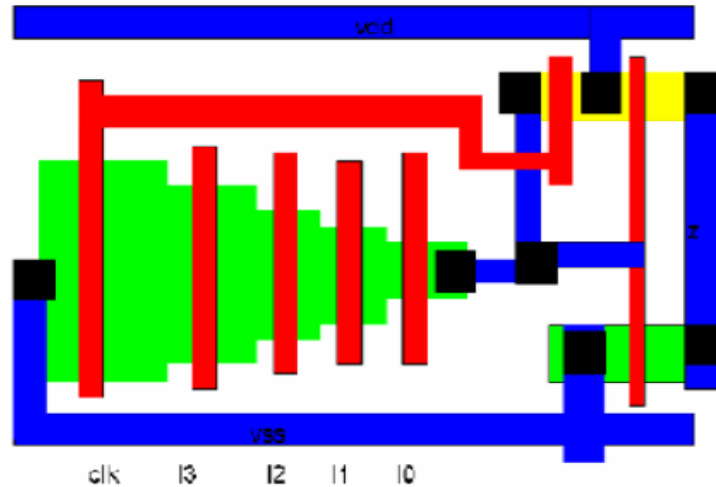


Figure 30: Layout optimization with varying diffusion areas.

2. Less optimized gates could occur even in the case of parallel connected transistors. This is usually seen in parallel inverters, nor & nand. When drains are connected in parallel, we must try and reduce the number of drains in parallel i.e. wherever possible we must try and connect drains in series at least at the output. This arrangement could reduce the capacitance at the output enabling good voltage levels. One example is as shown next.

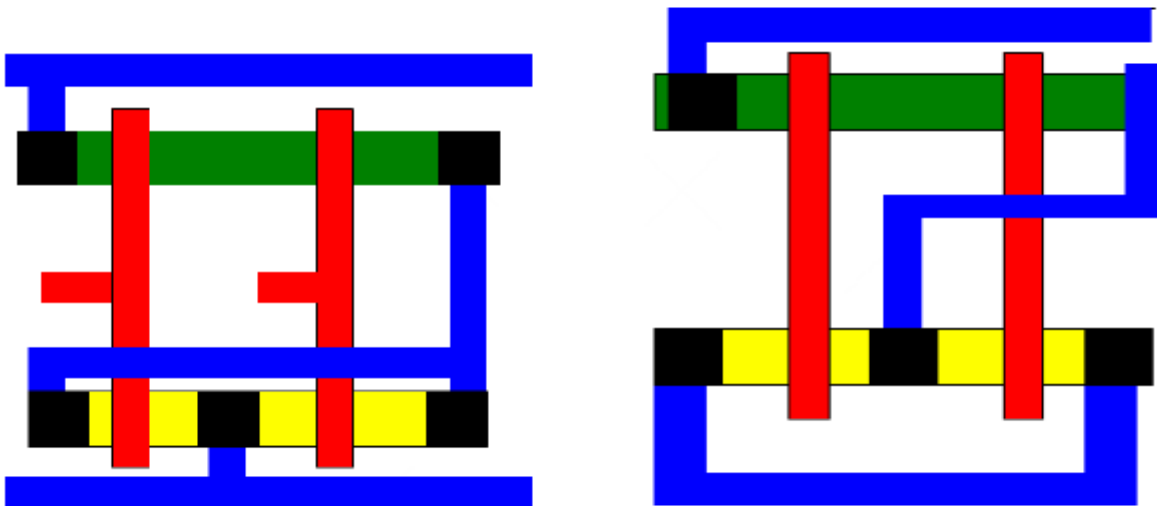


Figure 30: Layout of nor gate showing series and parallel drains.