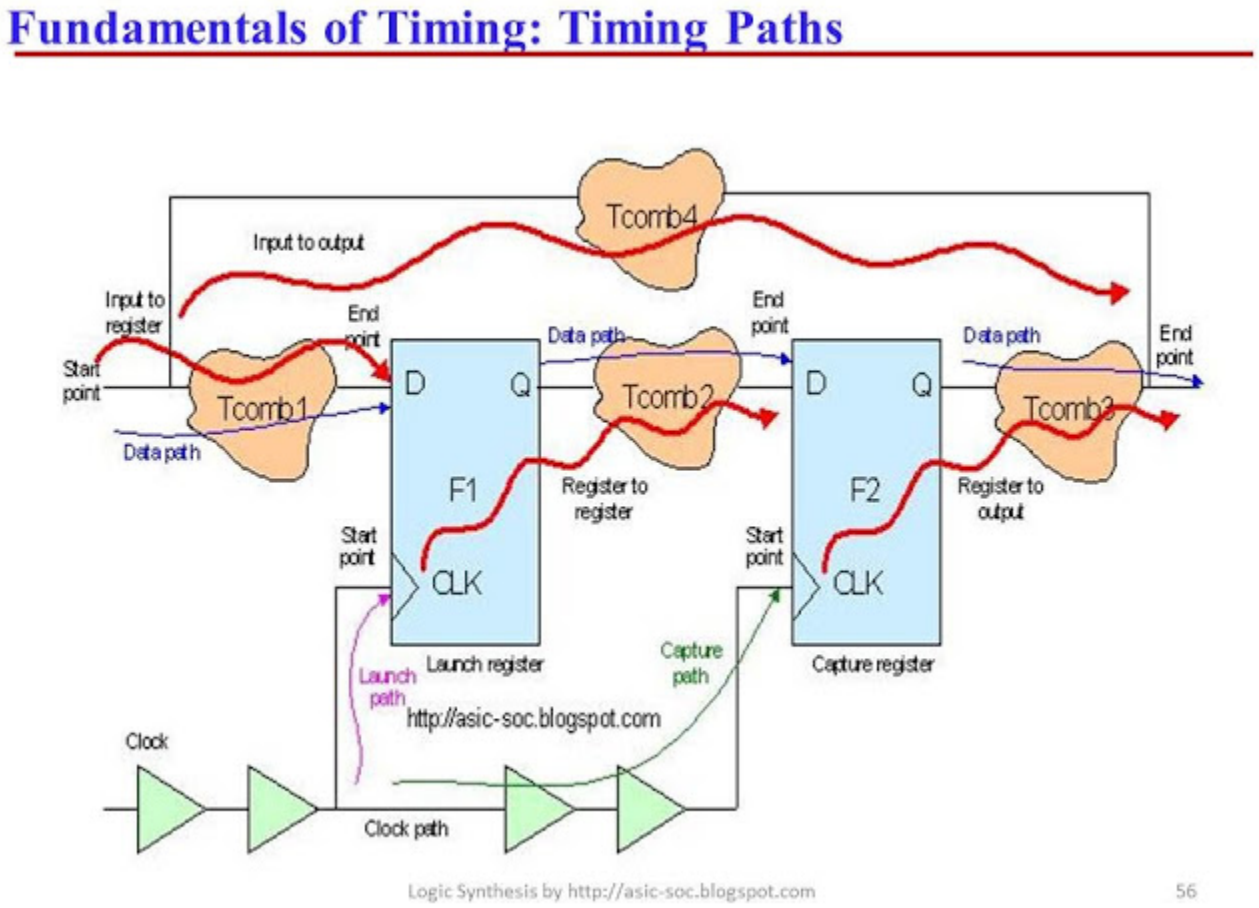
FUNDAMENTALS OF TIMING

11.1. Timing paths

Any digital circuit can be represented as a “timing path” modeled between two flip flops.



Timing Path

Timing path is defined as the path between start point and end point where start point and end point is defined as follows:

Start Point:

All input ports or clock pins of a sequential element are considered as valid start point.

End Point:

All output port or D pin of sequential element is considered as End point.

For Static Timing Analysis (STA) design is split into different timing path and each timing path delay is calculated based on gate delays and net delays. In timing path data gets launched and

traverses through combinational elements and stops when it encounter a sequential element. In any timing path, in general (there are exceptions); delay requirements should be satisfied within a clock cycle.

In a timing path wherein start point is sequential element and end point is sequential element, if these two sequential elements are triggered by two different clocks(i.e. asynchronous) then a common least common multiple (LCM) of these two different clock periods should be considered to find the launch edge and capture edge for setup and hold timing analysis.

Different Timing Paths

Any synchronous design is split into various timing paths and each timing path is verified for its timing requirements. In general four types of timing paths can be identified in a synchronous design. They are:

- Input to Register
- Input to Output
- Register to Register

Register to Output

Input to Output:

It starts at input port and ends at output port. This is pure combinational path. You can hardly find this in a synchronous design.

Input to Register:

Semi synchronous; Register is controlled by the clock. Input data can come at any time.

Register to Register:

Purely sequential; both starting and ending flops are controlled by the clock.

Register to Output:

Data can come at any point of time.

Clock path

The path wherein clock traverses is known as clock path. Clock path can have only clock inverters and clock buffers as its element. Clock path may be passed trough a “gated element” to achieve additional advantages. In this case, characteristics and definitions of the clock change accordingly. We call this type of clock path as “gated clock path”. The process of “clock gating” has main advantage of dynamic power saving.

Data path

The path wherein data traverses is known as data path. Data path is a pure combinational path. It can have any basic combinational gates or group of gates.

Launch path

Launch path is part of clock path. Launch path is launch clock path which is responsible for launching the data at launch flip flop.

Launch path and data path together constitute arrival time of data at the input of capture register.

Capture path

Capture path is part of clock path. Capture path is capture clock path which is responsible for capturing the data at capture flip flop.
Capture clock period and its path delay together constitute required time of data at the input of capture register.

Source : http://asic-soc.blogspot.in/2013/08/fundamentals-of-timing.html