FPGA-BASED CONTROL OF THERMOELECTRIC COOLERS FOR LASER DIODE TEMPERATURE REGULATION

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Abstract:
The proportional-integral-derivative (PID) controller is the most used controller in the industry. Field programmable gate arrays (FPGAs) allow efficient implementation of PID controllers. This paper presents the temperature regulation of a 48W laser diode through thermoelectric coolers (TECs). The temperature regulation system is designed and tested. The results demonstrate the feasibility and applicability of PID control through FPGA.

Keywords: FPGA; PID Controller; Thermoelectric Cooler; Laser Diode.

1. Introduction

The proportional-integral-derivative (PID) controller is the most used controller in dynamic systems. It is used for aerospace, industrial process control, robotics, automation, transportation and many other areas. The implementation of PID controller has evolved from early mechanical and pneumatic designs, to analog circuits thanks to the discovery of the transistors, and lately to micro-processor systems. The emergence of low cost, powerful micro-processors and digital signal processors (DSPs) made it possible for the digital control to become a competitive choice. Moreover, field programmable gate arrays (FPGAs) are capable to execute concurrent operations, allowing parallel architectural design of digital PID controllers [1, 2].

Implementation of PID controller in FPGA is not new. Previous work has reported the use of FPGAs in digital feedback systems for magnetic bearings [3], pulse-width modulation DC-to-AC converters [4], AC-to-DC converters [1], induction motors [5] and variable speed drives [6].

This paper is about the design and implementation of FPGA-based PID controller for thermoelectric coolers (TECs). These coolers regulate the operating temperature of a 48W laser diode.

This paper is organized as follows; section 2 gives a brief background of the thermoelectric principles and FPGA architecture. Section 3 explains the experimental setup of the laser diode temperature regulation. Section 4 shows the closed-loop response of the proposed system. Finally, general conclusions are made.

2. Background

2.1. Thermoelectric basic principles

TEC modules are solid state heat pumps used in applications where temperature stabilization, temperature cycling, or cooling below ambient are required. There are many products using TECs, including CCD cameras (charge coupled device), laser diodes, microprocessors, blood analyzers, portable picnic coolers and car seat coolers/heaters [7]. TECs have been widely used in military, aerospace, instrument, industrial and commercial

products [8-10]. They have been used for temperature control of lead acid batteries and climate control for EVs [11, 12] and for thermoelectric generation for hybrid vehicles [13].

TECs are based on the Peltier Effect, by which DC current applied across two dissimilar materials causes a temperature differential. The Peltier Effect is one of the three thermoelectric effects, the other two are known as the Seebeck Effect and Thomson Effect.

The typical thermoelectric module is manufactured using two thin ceramic wafers with a series of P and N doped bismuth-telluride semiconductor materials sandwiched between them. The ceramic material on both sides of the thermoelectric adds rigidity and the necessary electrical insulation. The thermoelectric couples are electrically in series and thermally in parallel. A thermoelectric module can contain one to several hundred couples.

As the electrons move from the P type material to the N type material, the electrons jump to a higher energy state absorbing thermal energy (cold side). Continuing through the lattice of material, the electrons flow from the N type material to the P type material dropping to a lower energy state and releasing energy as heat to the heat sink (hot side), as shown in Fig. 1.
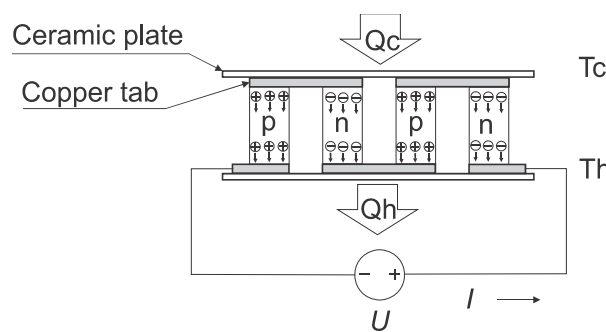

Figure. 1. Thermoelectric device

2.2. FPGA Architecture

The basic architecture of an FPGA consists of the following three elements:

(1). Configurable logic blocks (CLB): made of look-up-tables (LUT). The LUT with N-inputs acts as 2^N by 1 bit memory. The user can directly implement any N-input combinational function by entering its truth table into the LUT. A D flip-flop is added in order to implement sequential logic functions. A 4-input LUT is illustrated in Fig. 2
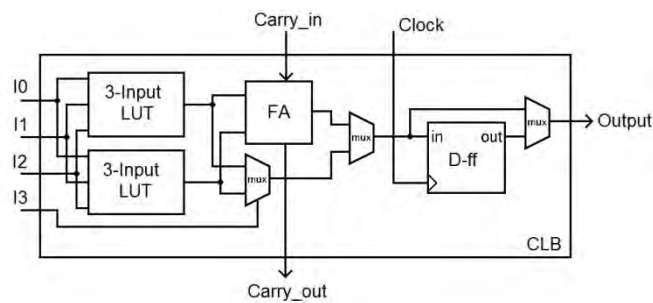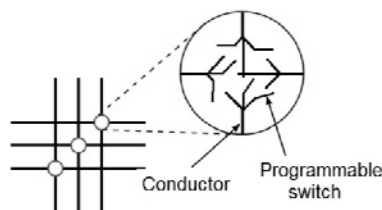

Figure 2: Configurable Logic Block

Figure 3: Interconnect resources.

(2). Input output blocks (IOB): provide the interface between the FPGA and the "outside word". They consist of tri-state buffers that enable the signal to act as input or output. The signal can also be stored in a flip-flop available within the IOB.

(3). Interconnect resources: allow the implementation of a complete digital system by providing a means of connecting individual circuits. They connect signals between adjacent CLBs, CLBs and I/O blocks, and provide long lines for clock signals (high fan-out and low-skew distribution). Fig. 3 illustrates I/O blocks.

3. Experimental testing of FPGA-based thermoelectric cooling of laser diode

3.1 Experimental set-up

Laser diodes are constructed of semiconductor materials; they produce very high heat loads. Optical efficiencies of these diodes are very dependent on operating temperature. Therefore precise temperature control is necessary. Conventional cooling systems for high-power diode arrays typically use liquid cooled approaches to maintain the diode temperature near room temperature.

Laser diodes using thermoelectric coolers (TECs) for precision temperature control is not a novel concept. TEC modules have shown to improve diode output levels and maintain wavelength integrity. A major trend for photonics in telecommunications has been the move to packaging that is smaller and less expensive.

The objective of this experimental procedure is to test the proposed FPGA-based PID controller. It is used to regulate the temperature of a 48W laser diode through TEC modules.

Fig. 4 shows the experimental set-up. A laser diode is first mounted in the middle of 100mm^2 aluminum-sheet. Then, four TEC modules of 30mm^2 are mounted on the sides of the aluminum sheet as shown in Fig. 4. Finally, four extruded heat sinks are mounted on the top of the TEC modules in order to extract the heat pumped by the TECs and the heat generated by the Joule effect. Fig. 5 shows the top and the side view of the installed laser diode.
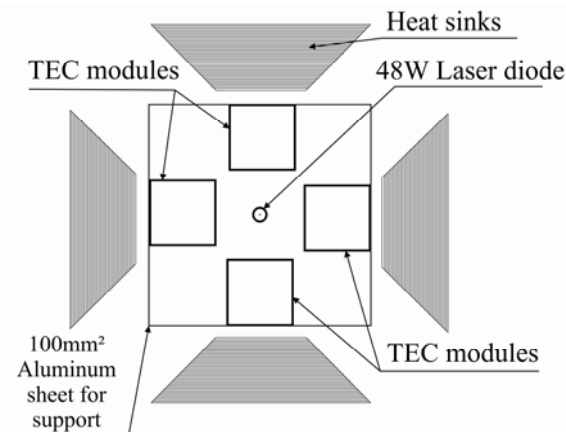

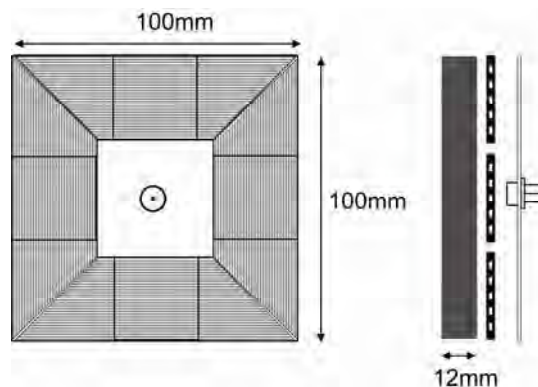Figure 4: Laser diode installation along with the TEC modules and heat sinks.

Figure 5: Top and side view of the installed laser diode.

Fig. 6 shows the block diagram of the proposed laser diode temperature regulation system. The FPGA chip hosts the comparator and the PID controller. The controller sends the output signal $u[n]$ to the bipolar driver circuit that makes the digital output signal from the FPGA suitable for the bipolar transistor. The bipolar transistor regulates the TEC modules input current. A thermocouple senses the operating temperature $T(t)$ and sends it to a 12-bit analog-to-digital converter to produce the quantized value of the temperature $T[n]$ and send it back to the FPGA chip. Finally, a subtracted produces the difference between the reference temperature $Tref[n]$ and the actual temperature $T[n]$.
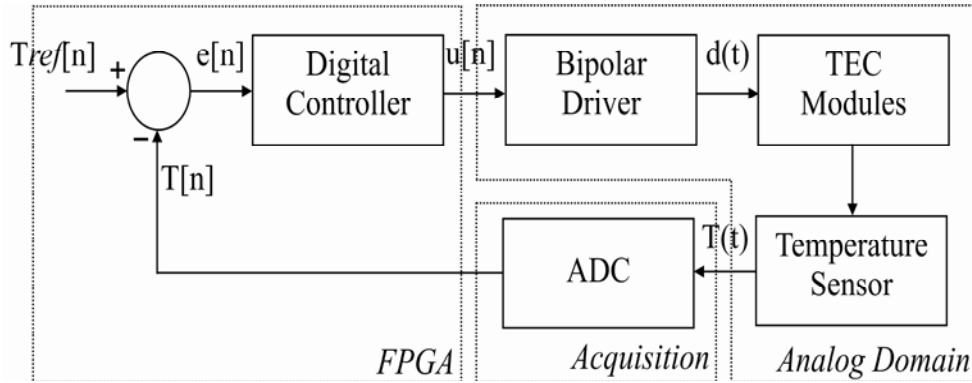

Figure 6 : Block diagram of the laser diode temperature regulation system

3.2 FPGA based PID Control

The PID control output is computed in continuous time in Eq. (1),

$$u(t) = k_p \left[e(t) + \frac{1}{T_i} \int_0^t e(t)\,dt + T_d \frac{de(t)}{dt} \right] \qquad (1)$$

where k_p is the proportional gain, T_i is the reset time and T_d is the derivative time. In discrete time, it is possible to compute the actual output $u[n]$ based on past output $u[n-1]$ and the correction term $\Delta u[n]$ according to Eq. (2) to eq. (4).

$$\Delta u[n] = u[n] - u[n-1] \qquad (2)$$

$$u[n-1] = k_p\, e[n-1] + k_i \sum_{j=0}^{n-1} e[j] + k_d \{e[n-1] - e[n-2]\} \qquad (3)$$

$$u[n] = u[n-1] + (k_p + k_i + k_d)e[n] - (k_p + 2k_d)e[n-1] + k_d\, e[n-2] \qquad (4)$$

$$u[n] = u[n-1] + k_o\, e[n] + k_1 e[n-1] + k_2 e[n-2] \qquad (5)$$

In order to implement equation (5) in FPGA, it should be decomposed into accumulation and multiplication based operations. Three multiplications and four accumulations are needed as shown in equations (6) to (12), where p_c is the controlled variable, p_c is the set point and p_0, p_1, p_2, S_1, S_2 and S_3 are variables stored in temporary registers. Fig. 7. shows the architecture of the PID controller, where T is a saturation element.

$$e[n] = p_c + (-p_d) \qquad (6)$$
$$p_0 = k_0 e[n] \qquad (7)$$
$$p_1 = k_1 e[n-1] \qquad (8)$$
$$p_2 = k_2 e[n-2] \qquad (9)$$
$$S_1 = p_1 + p_2 \qquad (10)$$

$$S_2 = p_0 + S_1 \tag{11}$$
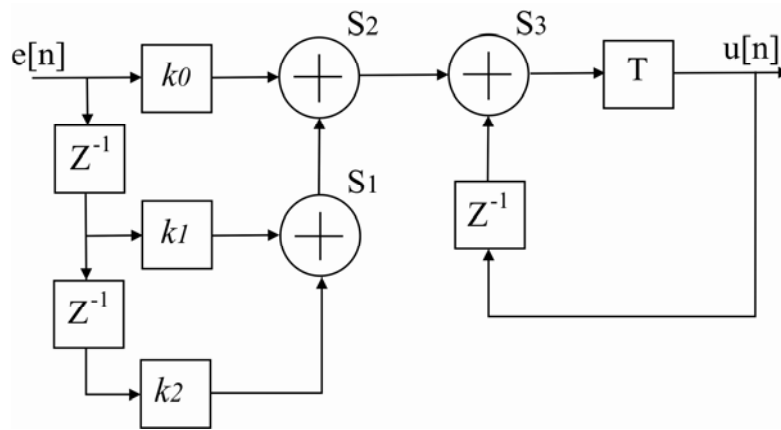
$$S_3 = u[n] = u[n-1] + S_2 \tag{12}$$

Figure 7: HDL Structural description of PID controller

3.3 Acquisition

The analog-to-digital converter (ADC) is responsible for the sampling and the quantization of the temperature value delivered by the temperature sensor. This temperature value must be in digital format useful for the subtracter and the PID controller. Eq. (13) shows the minimum number of bits required to sense the operating temperature.

$$n = \text{int}\left(\log_2 \left(\frac{V_{ADC\,(fs)}}{\beta.\Delta V_{Temp\,(\max)}} \right) \right) \tag{13}$$

where $V_{ADC\,(fs)} = 12V$ is ADC full scale voltage, $\beta = 1V\,/\,^\circ C$ is the temperature sensor gain and $\Delta V_{temp\,(\max)} = 0.003\,^\circ C$ is the maximal temperature variation allowed to be undetected. The needed resolution is then $n = 12$ bits.

4. Experimental testing and results

Fig. 8 shows the open-loop response and the closed-loop response of the cooled aluminum plate. This response was obtained with the following PID coefficients: $k_p = 10$, $k_i = 0.1, k_d = 50$. In open-loop response, the system takes about 90 seconds to settle to the reference value. In closed-loop response, it took about 19 seconds while having negligible over-shoot values.
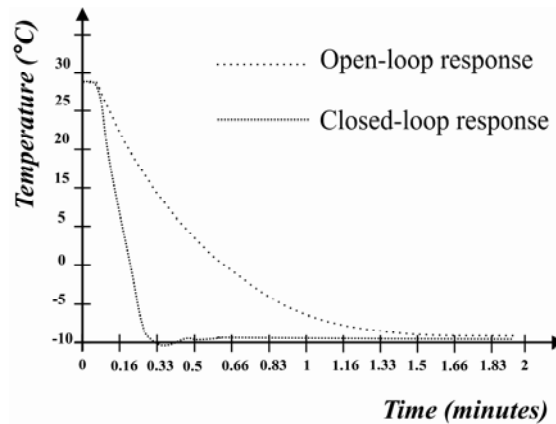
Figure 8: Open-loop and closed loop cooling system response

5. Conclusions

In this paper, an FPGA-based PID digital feedback control system was designed and tested. A 48W laser diode was mounted with Peltier thermoelectric coolers in which the temperature response was regulated by the proposed PID controller. It was noticed that the FPGA-based PID controller is effective in decreasing overshoot, oscillations and settling time, and has a fast response time. This paper shows the applicability of FPGA technology for process control.

References

[1]   P. Zumel, A. deCastro, O. Garcia, T. Riesgo, and J. Uceda, "Concurrent and simple digital controller of an AC/DC converter with power factor correction, " in Proc. IEEE Appl. Power Electron. Conf. Expo., 2002, vol.1, pp. 469–475.
[2]   L.Charaabi, E.Monmasson, and I. Slama-Belkhodja, "Presentation of an efficient design methodology for FPGA implementation of control systems: Application to the design of an antiwind-up PI controller," in Proc. IEEE Ind. Electron. Soc. Annu. Conf., Nov. 2002, vol.3, pp.1942–1947.
[3]   F. Krach , B. Frackelton , J. Carletta , and R. Veillette , "FPGA-based implementation of digital control for a magnetic bearing," in Proc. Amer. Control Conf., Jun. 2003, vol.2, pp.1080–1085.
[4]   S. L. Jung, M. Y. Chang, J. Y. Jyang, L.C. Yeh, and Y.Y. Tzou, "Design and implementation of an FPGA-based control IC for AC-voltage regulation, "IEEE Trans. Power Electron., vol.14, no.3, pp.522–532, May1999.
[5]   S. Ferreira, F. Haffner, L.F. Pereira, and F.Moraes, "Design and proto-typing of direct torque control of induction motors in FPGAs, " in Proc. IEEE Symp. Integr. Circuits and Syst. Des., Sep. 2003, pp.105–110.
[6]   F. Ricciand H. Le-Huy, "An FPGA-based rapid prototyping platform for variable-speed drives," in Proc. IEEE Ind. Electron. Soc. Annu. Conf., Nov. 2002, vol. 2, pp. 1156–1161.
[7]   R. Chein and G. Huang, "Thermoelectric cooler application in electronic cooling", Applied Thermal Engineering, vol. 24, pp. 2207–2217, Oct. 2004.
[8]   R.E Simons and R.C Chu, "Application of thermoelectric cooling to electronic equipment: a review and analysis", Sixteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium, pp. 1–9, 21–23 Mar 2000.
[9]   C. Alaoui and Z. M. Salameh, "Solid state heater cooler: design and evaluation", Large Engineering Systems Conference on Power Engineering, LESCOPE '01. Jul 11-13 2001, pp: 139-145.
[10] C. Alaoui, "Peltier Thermoelectric Modules Modeling and Evaluation", International Journal of Engineering, Vol. 5,   Issue: 1, March / April 2011, pp: 114-121.
[11] C. Alaoui and Z. M. Salameh, "A novel thermal management for electric and hybrid vehicles". IEEE Transactions on Vehicular Technology, vol. 54, pp. 468–476, Mar. 2005.
[12] C. Alaoui and Z. M. Salameh, "Modeling and simulation of a Thermal Management System for Electric Vehicles". The 29th Annual Conference of the IEEE Industrial Electronics Society, 2003. IECON '03. 2-6 Nov. 2003, pp: 887 – 890.
[13] X. Zhang, K. T. Chau and C. C. Chan, "Overview of Thermoelectric Generation for Hybrid Vehicles", Journal of Asian Electric Vehicles, vol. 6, No. 2, pp. 1119–1124, 2008.