

FPGA Implementation of OFDM Transceiver using FFT Algorithm

Shaminder Kaur¹, Rajesh Mehra²

¹ ME Student, ECE Department, NITTTR, Chandigarh, India-160019

² Associate Professor, ECE Department, NITTTR, Chandigarh, India-160019
er.shaminderkaur@gmail.com

Abstract- Orthogonal Frequency Division Multiplexing (OFDM) is the most promising modulation technique. It has been adopted by most wireless and wired communication standards. The idea is to utilize a number of carriers, spread regularly over a frequency band, in such a way so that the available bandwidth is utilized to maximal efficiency. In this paper the design and implementation of OFDM on a Field Programmable Gate Array (FPGA) device has been presented. This attractive architecture uses Radix-2 serialized 512-point FFT (Fast Fourier Transform) algorithm that enhances its speed. The system design is optimized in terms of both area and speed. The implementation was made on FPGA since it allows flexibility in design and also it can achieve higher computing speed than digital signal processors. ASIC-like performance with lower development time and risks can also be achieved. The results show that the design has been simulated up to 227.355 MHz and it achieves higher speed and lower area.

Keywords: FFT, FPGAs, OFDM, pipelining, Radix-2, VHDL.

1. INTRODUCTION

The principles of OFDM have been in existence for several decades. However, in recent years these techniques came into practice in modern communications system. In 4G wireless communication systems, bandwidth is a precious commodity, and service providers are continuously met with the challenge of accommodating more users with in a limited allocated bandwidth. Orthogonal frequency division multiplexing (OFDM) is such a technique which provides an efficient means to handle high speed data streams on a multipath fading environment that causes ISI. The required bit rates are achieved due to OFDM multicarrier transmissions. OFDM systems perform better than single carrier systems particularly in frequency selective channels. It is a multiplexing/multiple access scheme that has many favorable features required for the fourth generation systems [1, 2]. FFT (Fast Fourier Transform)/ (Inverse Fast Fourier Transform) IFFT are the main blocks in OFDM system. They are important in achieving high speed signal processing. FFT helps to transform the signal from time domain to frequency domain where filtering and correlation can be performed with fewer operations [3, 4].

It is important to note that the FFT/IFFT algorithms should be chosen to consider the execution speed, hardware complexity, flexibility and precision [5]. Nevertheless, for real time systems the execution speed is the main concern [6] - [8]. The observation made on various architectures reveals that most of the existing work has been based on design and implementation of the transmitter and limited work has been done on the complete design of OFDM transceiver. The OFDM hardware implementation has been done either on ASICs, Virtex based FPGA [9] - [11]. ASIC based designs suffer from more time to market factor, high cost and provide less flexibility. Moreover, DSP based designs can only support limited data rates due to lack of parallelism and also they have less number of MAC(multiply and accumulate) units. On the other hand, the modern programmable circuits like an FPGA provides parallel processing system, putting the FPGA computing speed at a significant advantage over DSPs [12] - [14].

This paper presents the implementation of OFDM Transceiver on FPGA. It has also been observed that most of the existing work has been done on either speed or area. Speed has been enhanced at the cost of area and high cost FPGAs like Virtex4. Resource consumption has been reduced by degradation in speed [15, 16]. So still a number of challenges are there which needs to be researched upon. In order to meet these challenges there is an urgent need to optimize both speed and area simultaneously in order to provide optimum solution for wireless communication. By keeping in mind the existing gaps and needs of today's wireless communication systems, the main objective of this work is to design an OFDM Transceiver system on a low cost FPGA like Spartan3E or Virtex2 Pro to improve speed and area simultaneously, by utilizing optimal number of resources in terms of slices, LUTs and multipliers of target FPGA to provide high performance cost effective solution for wireless communication applications.

2. OFDM Basics

OFDM is a wideband wireless digital communication technique that is based on block modulation. It is known as block modulation because the OFDM frame is split into blocks and each block has T_s duration. These blocks contain one or more symbols. Each symbol or group of symbols will be assigned a separate carrier. The OFDM arranges the subcarriers in such a way that they do not overlap and maintain the orthogonality between them. These subcarriers are modulated independently. All the split information is then transmitted in parallel through multiple carriers [17]. In OFDM the carriers can be placed as near as possible maintaining the orthogonality, thereby making better utilization of the spectrum. The width of the pulse puts the limit on the sub-carrier spacing. The subcarrier spacing will be inversely proportional to the symbol duration, where symbol duration is denoted by T_s . Longer is the symbol duration, better is the performance [18].

Orthogonal frequency division multiplexing (OFDM) is also very effective technique to mitigate inter-symbol interference (ISI) in handling time dispersion of multipath fading channels. This is the fundamental problem for communication systems. OFDM also prevents ICI (inter carriers interference) by making all the subcarriers orthogonal to each other [19]. OFDM is a special case of multicarrier transmission in which a single information bearing stream is transmitted over many lower rate sub channels. It has various applications in optical communication also. It has been recently proposed for use in radio-over-fiber based links, in free space optical communication, in long haul optical communication systems, in multimode fiber links etc. For understanding the OFDM operation, it is essential to understand the concept of orthogonality. *Orthogonality* is defined for both real and complex valued functions. As shown in eq. 1 the two functions $\alpha_m^*(t)$ and $\alpha_n(t)$ are said to be orthogonal with respect to each other over the interval $a < t < b$ if they satisfy the condition:

$$\int_a^b \alpha_m^*(t) \alpha_n(t) dt = 0, n \neq m \quad (1)$$

Orthogonality is also defined as the two coexisting signals are independent of each other in specified time interval and do not interact with each other as shown in fig 2.3. Here the six sub carriers are placed orthogonally such that the peak of one subcarrier occurs when other subcarriers are at zero. This is achieved practically with help of Inverse Fast Fourier Transform (IFFT) technique. Orthogonality is a property that allows multiple information signals to be transmitted perfectly over a common channel, thereby making better spectrum utilization. The signal is detected without interference. Ultimately ISI is conquered. Loss of orthogonality results in blurring between the information signals and degradations in communications. Two periodic signals are orthogonal when the integral of their product, over one period, is equal to zero and they have integral number of cycles in the fundamental period. Orthogonality of subcarriers is crucial for OFDM system. If orthogonality is destroyed, the receiver will have a serious bit error rate due to (ICI). A cyclic extension of the signal in time domain called cyclic prefix (CP) is inserted between each OFDM symbol to eliminate ISI almost completely for it is larger than maximum of time delay, which keeps orthogonality between each subcarriers as well [20, 21].

3. Proposed OFDM Transceivers its Simulation

The proposed design has been presented in this section. Figure 1 shows the diagram of proposed OFDM design. Radix-2 serialized FFT algorithm is used. The FFT block implements the Decimation-in-Time (DIT) FFT algorithm. It is composed of 9 stages of radix-2 butterfly units. These FFT stages are pipelined which further enhances its speed and is simulated up to 227.355 MHz frequency. A serial FFT implemented in this model uses only one butterfly resource for each stage of implementation. With help of this area factor is also taken care of. Hence there is an optimized design in terms of both speed and area. As shown in the fig. 1, the proposed design consists of various stages. QAM modulator modulates the signal using QAM (Quadrature amplitude modulation). QAM block is followed by insert pilot block. To generate OFDM successfully, some additional subcarriers, called pilot subcarriers, are added to create the reference at the receiver end, which carries out the channel estimation procedure to remove channel impairments.

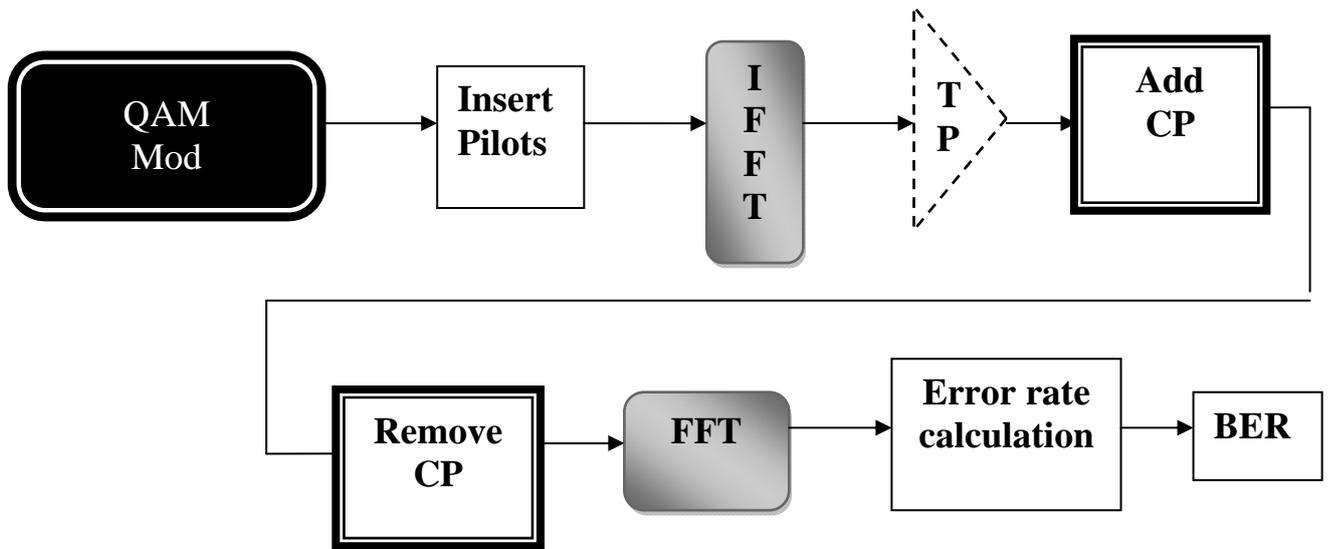


Fig.1. OFDM Model using FFT Algorithm

Since the effective SNR is reduced by transmitting pilots, the spacing of the pilots is a trade-off between good channel estimation and high effective SNR. Pilot means reference signal used by both transmitters and receivers. In order to perform frequency domain data into time domain data, IFFT block is used. Inverse Fast Fourier Transform (IFFT) correlates the frequency domain input data with its orthogonal basis functions, which are sinusoids at certain frequencies. This correlation is equivalent to mapping the input data onto the sinusoidal basis functions. It provides complete spectrum setting. The FFT and IFFT are the most important blocks in the OFDM system and their performances have a big effect on the whole system. IFFT increase the speed of processing and decrease the computational complexity. IFFT scales the signal power down by IFFT size N, so it degrades bit error rate (BER). Hence in order to improve BER power scaling block is used. It improves the BER (bit error rate). The **ISI** is a common problem found in high data rate communication. It occurs when the transmission interferes with itself and the receiver cannot decode the transmission correctly. This is because as the data rate increases, the time duration between the consecutive pulses decreases. For avoiding ISI, the pulse time duration should be greater than the maximum delay of the channel. The ISI is one of the major drawbacks of multipath single-carrier transmission. To avoid this, guard interval is provided along with the data period so that the ISI effect observed in the guard interval can be removed afterwards and the data can be retrieved.

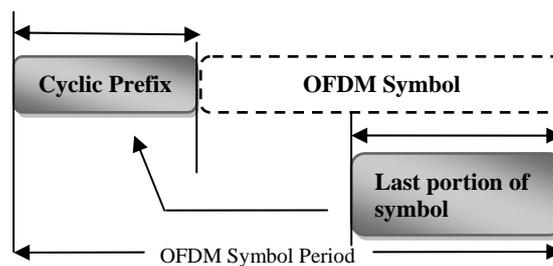


Fig.2 Elimination of ICI/ISI with addition of Cyclic prefix

It is depicted in the figure 2 that by greatly increasing the symbol period the fading per subcarrier becomes flat, so that it can be equalised with a single coefficient per subcarrier. The addition of cyclic prefix eliminates Intersymbol Interference (ISI) due to multipath. As shown in the fig.3 FFT transforms time domain signal into frequency domain. The receiver basically does the reverse operation to the transmitter. The FFT of each OFDM symbol is performed to find the original transmitted spectrum. The phase angle of each transmission carrier is then evaluated and converted back to the data word by demodulating the received phase (demapping). The data words are then split back to the same pattern as the original bits to have the serial data again by parallel-to-serial conversion.

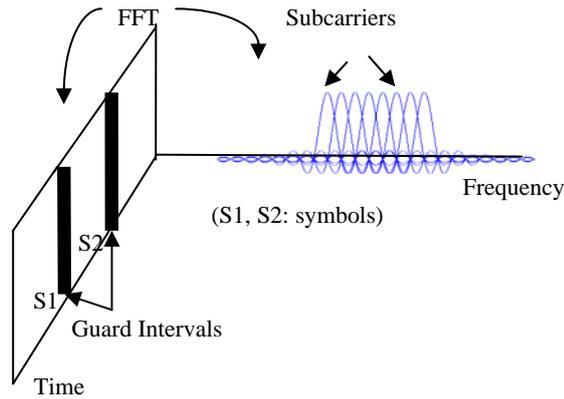


Fig.3 Description of FFT Block

The next block is used to calculate the bit error rate which is the number of bit errors divided by the total number of transferred bits during a studied time interval. BER is a unit less performance measure, often expressed as a percentage. The waveform obtained have been investigated and found in conformity with the theoretical observations. Waveform obtained has been presented in Fig.4.

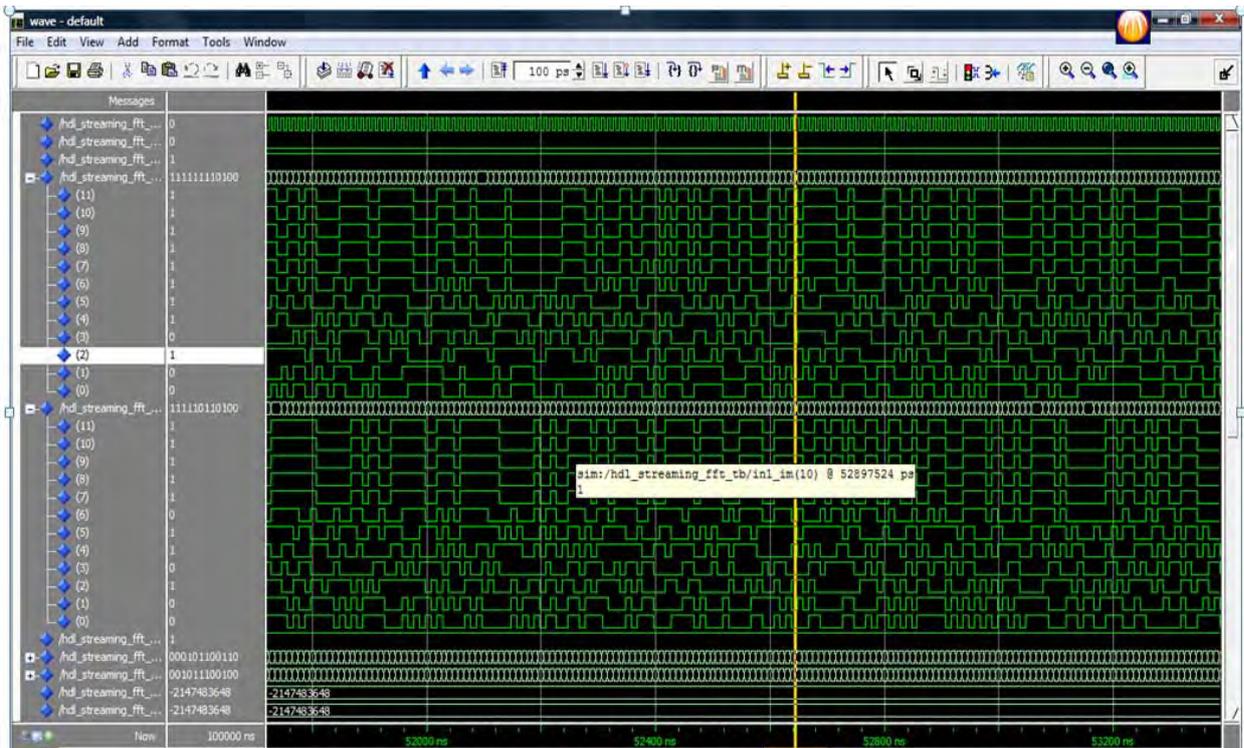


Fig.4. Simulated waveform

The above waveform is Modelsim simulated waveform. VHDL code has been developed and simulated using Modelsim where the output is shown in fig.4. The real and imaginary parts are shown in the figure above. When the test pattern 111110110100 is entered at the transmitter side, the same has been recovered at the receiver side as shown in the figure 4.

TABLE 1
Hardware Utilization Report with Virtex2 as Target Device

Logic Utilization	Used	Available	Utilization
Number of Slices	2598	13696	18%
Number of Slice Flip Flop	4305	27392	15%
Number of 4 input LUT's	2734	27392	9%
Number of bonded IOBs	52	556	9%
Number of BRAMs	11	136	8%
Number of MULT18X18s	32	136	23%
Number of GCLKs	1	16	6%

TABLE 2
Comparison Table

Logic Utilization	Proposed Design (Virtex2 Pro)	OFDM Design[1] (Virtex2 Pro 2VP30fg676)
Frequency (Speed Factor)	227.355MHz	100MHz
No. of Slices/CLB Slices(Area Factor)	2598	3418
No. of MUL (Area Factor)	32	58
No. of Bounded IOB's	52	34

4. Hardware Implementation

The proposed design has been synthesized and implemented on Virtex-2 Pro xc2vp30-5ff896 based device. The model was made in simulink. VHDL code has been generated and simulated using Modelsim program. The XST synthesis tool has been used to synthesis the model and it has allocated following resources (table 1): 2598 Slices (18%), 4305 Flip Flops (15%) and 2734 LUTs (9%) out of available on target device. The results show that the design has been simulated up to 227.355 MHz and it achieves higher speed and lower area by using Radix-2 serialized 512 point FFT algorithm. In this work DIT algorithm is used. Each FFT stage i.e. radix 2 FFT stage include one radix 2 butterfly computing unit, memory blocks to cache the streaming data, ROM to store FFT twiddle factors, control logic. The memory size of each stage equals the stage number. Here only one butterfly resource is used for each stage because of serial FFT implementation instead of 4 butterfly resources in case of typical 8-point FFT. This increases its speed and area factor is also taken care of. The speed, area and cost factor of the proposed design and OFDM design [1] has been compared which is shown in table 2. The maximum frequency for the proposed design is 227.355 Mhz as compared to OFDM design [1]. It can be observed from the table 2 that the proposed design has more speed as compared to the design [1]. The occupied area of an FPGA is proportional to number of used multipliers. The proposed design uses 32 multipliers as compared to OFDM design [1].The proposed design has shown improvement in area factor also in terms of no. of slices and no. of multipliers. Moreover the proposed design has been implemented on multipliers based lower end FPGAs in order to provide cost effective solution for wireless communication applications.

5. Conclusion

An area and speed efficient technique using FPGA has been proposed to OFDM so that it can be efficiently used in wireless communication application. The concept of Radix-2 serialized FFT (DIT) algorithm has been introduced to enhance the speed and area efficiency. The comparison with other model reveals the speed and area of our model. The developed OFDM has been hardware implemented on Virtex-2Pro based xc2vp30-5ff896 target device using Xilinx ISE (10.1) tool. The required minimum input arrival time before clock is 7.183ns and the maximum output required time after clock is 5.366ns. The results show that the developed OFDM can operate at maximum frequency of 227.355 MHz by consuming very less number of resources to provide cost effective and high performance solution for wireless communication applications.

6. References

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