ENHANCEMENT TYPE MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

Basic Construction

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

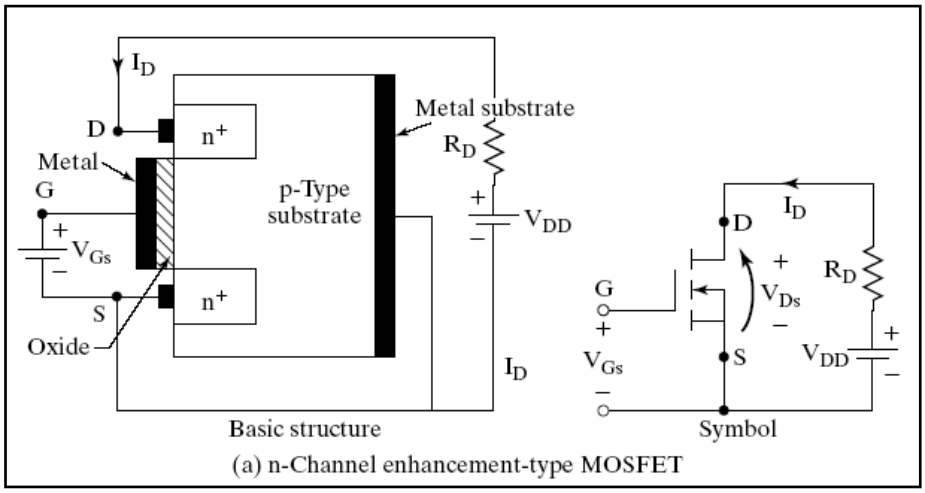


Fig. 2.17: Structure of n-channel enhancement type MOSFET

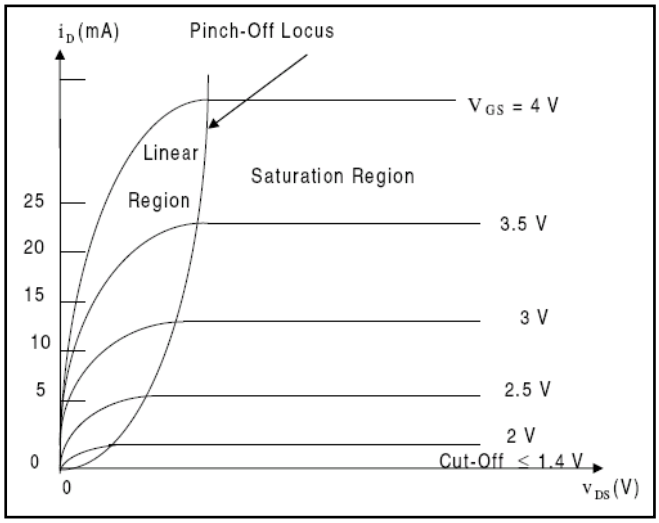
Operation

If $V_{GS} = 0V$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased p-n junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

The level of V_{GS} that result in significant increase in drain current is called threshold voltage V_T. As V_{GS} increases the density of free carriers will increase resulting in increased level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

Drain Characteristics



Transfer Characteristics