

ENHANCEMENT MODE MOSFET

Types of FETs

The family of FETs may be divided into :

- (i) Junction FET
- (ii) Depletion Mode MOSFET
- (iii) Enhancement Mode MOSFET

(i) JFET Definition

•**JFET** is a unipolar-transistor, which acts as a voltage controlled current device and is a device in which current at two electrodes is controlled by the action of an electric field at a reversed biased p-n junction.

(ii) Enhancement Mode MOSFET

The Insulated Gate FET (IGFET).

The Metal Oxide Silicon FET (MOSFET) or Metal Oxide Silicon Transistor (M.O.S.T.) has an even higher input resistance (typically 10^{11} to 10^{15} ohms) than that of the JFET. In the MOSFET device the gate is completely insulated from the rest of the transistor by a very thin layer of metal

oxide (Silicon dioxide SiO_2). Hence the general name applied to any device of this type, is the IGFET or Insulated Gate FET.

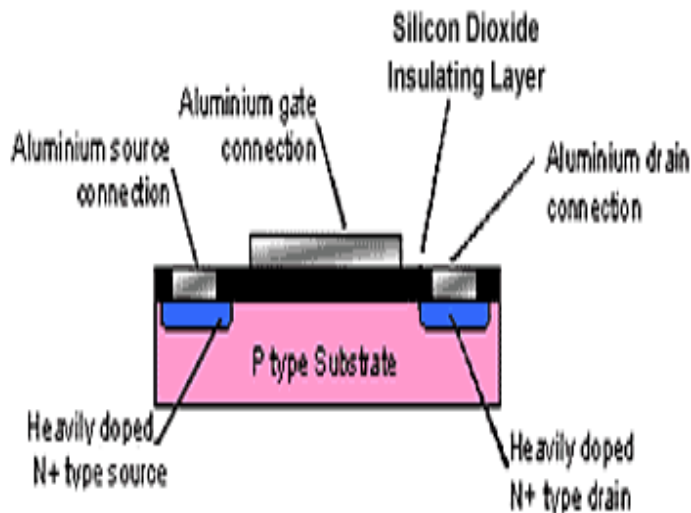


Fig. 1.8 Construction of a N Channel Enhancement Mode MOSFET

The basic construction of a MOSFET is shown in Fig. 1.8. A body or substrate of P type silicon is used, then two heavily doped N type regions are diffused into the upper surface, to form a pair of closely spaced strips.

A very thin (about 10^{-4} mm) layer of silicon dioxide is then evaporated onto the top surface forming an insulating layer. Parts of this layer are then etched away above the N type regions using a photographic mask to leave these regions uncovered. On top of the insulating layer, between the two N type regions, a layer of aluminum is deposited. This acts as the GATE electrode. Metal contacts are also deposited on the N type regions, which act as the SOURCE and DRAIN connectors.

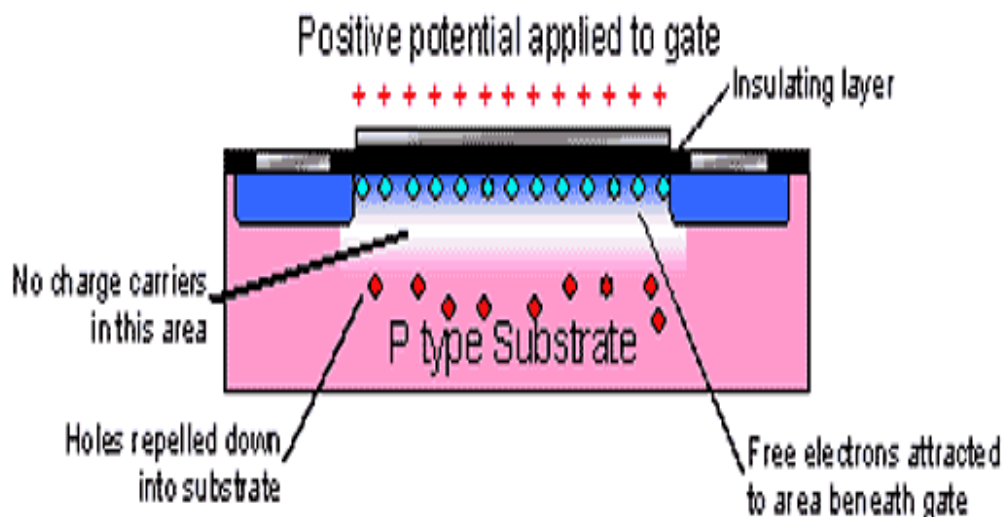


Fig.1.9 Enhancement Mode Operation.

The gate has a voltage applied to it that makes it positive with respect to the source. This causes holes in the P type layer close to the silicon dioxide layer beneath the gate to be repelled down into the P type substrate, and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode (they can't reach the gate because of the insulating silicon dioxide layer) bridging the gap between the heavily doped source and drain areas. This

layer is sometimes called an "inversion layer" because applying the gate voltage has caused the P type material immediately under the gate to firstly become "intrinsic" (with hardly any charge carriers) and then an N type layer within the P type substrate.

Any further increase in the gate voltage attracts more charge carriers into the inversion layer, so reducing its resistance, and increasing current flow between source and drain. Reducing the gate source voltage reduces current flow. When the power is switched off, the area beneath the gate reverts to P type once more.

As well as the type described above, devices having N type substrates and P type (inversion layer) channels are also available. Operation is identical, but of course the polarity of the gate voltage is reversed.

This method of operation is called "ENHANCEMENT MODE" as the application of gate source voltage makes a conducting channel "grow", therefore it enhances the channel. Other devices are available in which the application of a bias voltage reduces or "depletes" the conducting channel.

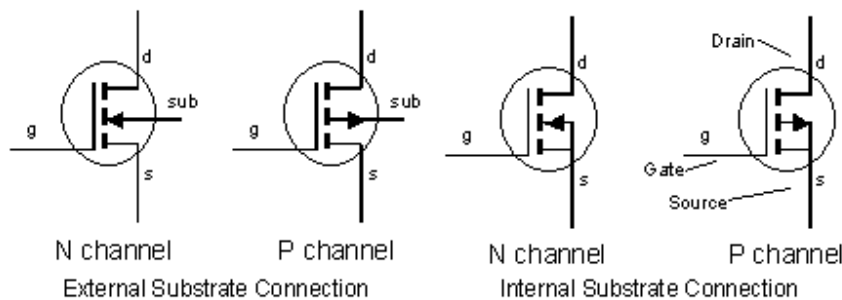


Fig. 1.10 Circuit Symbols for Enhancement Mode MOSFETs (IGFETs)

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