

# ENCODING FOR BJT AND MOSFETS





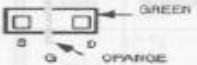
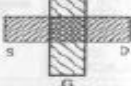

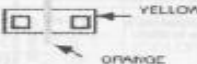



COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE	MONOCHROME	Polysilicon 2	MONOCHROME	CPS
SEE COLOR PLATE 1(2)		Bipolar npn transistor	see Figure 3-19(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor		CCA
			n-well	
FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)	
<i>n</i> -type enhancement poly 2 transistor				
Transistor length to width ratio L:W may be shown.				
<i>p</i> -type enhancement poly 2 transistor				
Note: <i>p</i> -type transistors are placed above and <i>n</i> -type transistors below the demarcation line.				
npn bipolar transistor			See Figure 3-19(f) and Color plate 6	

Figure 3: Bi CMOS encodings.

There are several layers in an nMOS chip:

- \_ a p-type substrate
- \_ paths of n-type diffusion
- \_ a thin layer of silicon dioxide
- \_ paths of polycrystalline silicon
- \_ a thick layer of silicon dioxide
- \_ paths of metal (usually aluminum)
- \_ a further thick layer of silicon dioxide

With contact cuts through the silicon dioxide where connections are required. The three layers carrying paths can be considered as independent conductors that only interact where polysilicon crosses diffusion to form a transistor. These tracks can be drawn as stick diagrams with \_ diffusion in green \_ polysilicon in red \_ metal in blue using black to indicate contacts between layers and yellow mark regions of implant in the channels of depletion mode transistors.

With CMOS there are two types of diffusion: n-type is drawn in green and p-type in brown. These are on the same layers in the chip and must not meet. In fact, the method of

fabrication required that they be kept relatively far apart. Modern CMOS processes usually support more than one layer of metal. Two are common and three or more are often available.

Actually, these conventions for colors are not universal; in particular, industrial (rather than academic) systems tend to use red for diffusion and green for polysilicon. Moreover, a shortage of colored pens normally means that both types of diffusion in CMOS are colored green and the polarity indicated by drawing a circle round p-type transistors or simply inferred from the context. Colorings for multiple layers of metal are even less standard.

There are three ways that an nMOS inverter might be drawn:

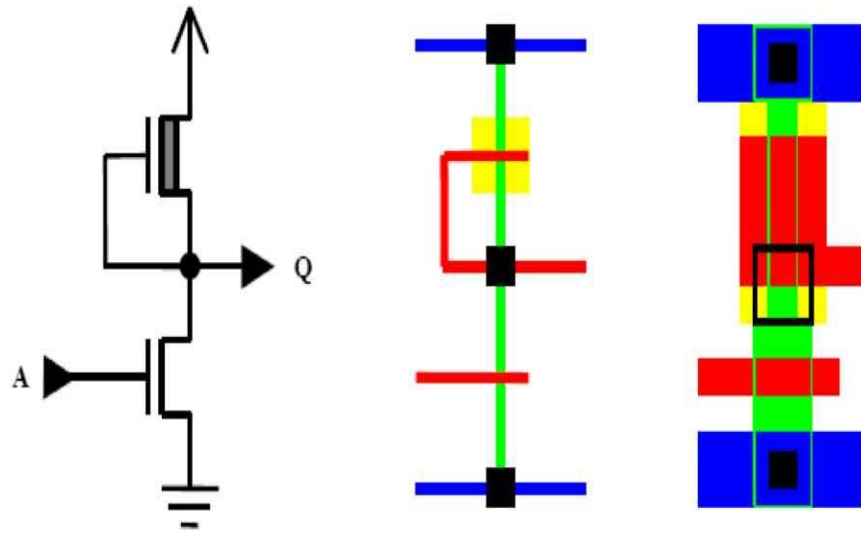


Figure 4: nMOS depletion load inverter.

Figure 4 shows schematic, stick diagram and corresponding layout of nMOS depletion load inverter

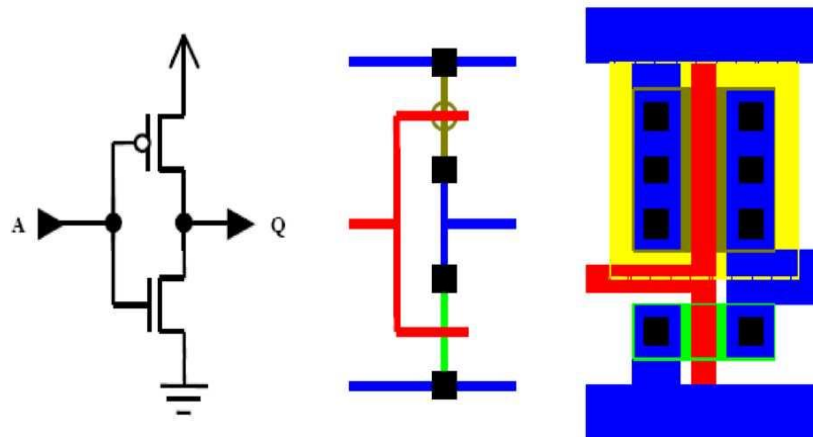


Figure 5: CMOS inverter

Figure 5 shows the schematic, stick diagram and corresponding layout of CMOS inverter.

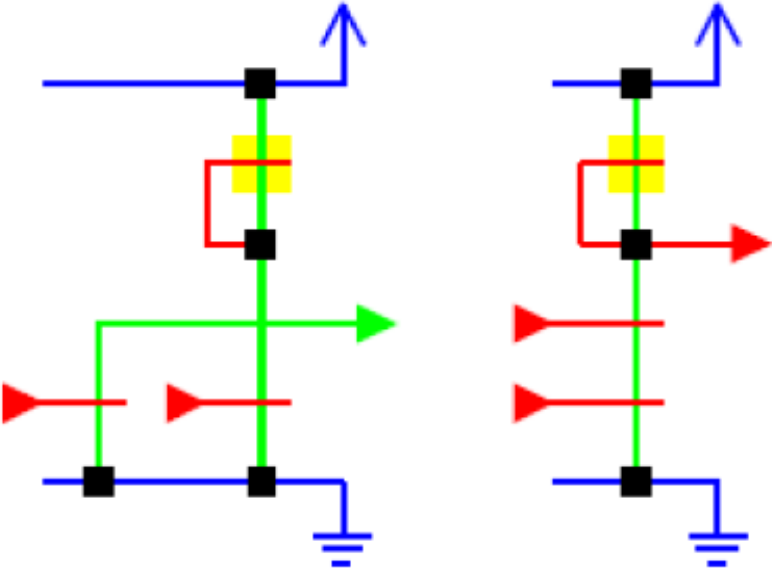


Figure 6 shows the stick diagrams for nMOS NOR and NAND.

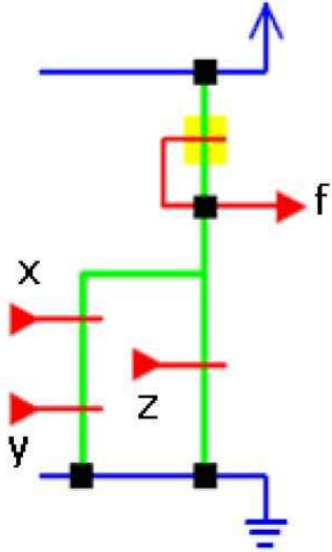


Figure 7: stick diagram of a given function f.

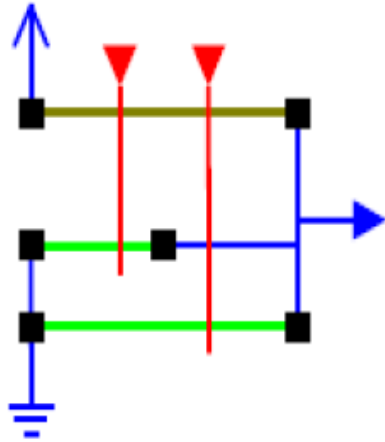


Figure 7

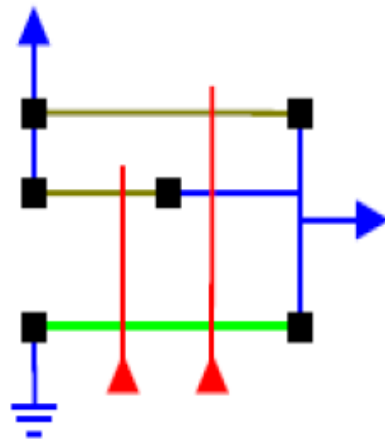


Figure 8

Figure 7 shows the stick diagram nMOS implementation of the function  $f = [(xy) + z]'$ .

Figure 8 shows the stick diagram CMOS NOR and NAND, where we can see that the p diffusion line never touched the n diffusion directly, it is always joined using a blue color metal line.

Source : <http://elearningatria.files.wordpress.com/2013/10/ece-v-fundamentals-of-cmos-vlsi-10ec56-notes.pdf>