Electronics Materials-Stress caused by thermal mismatch

The point was well made in the early 1970s by David Boswell that surface mount assemblies have many issues in common with civil engineering. For example, although there are major differences in scale and dimensions, the stress analysis of a chip component mounted at opposite ends has parallels with the stresses imposed by the environment on a bridge, and there are benefits from thinking in terms of the ability of both structures to withstand those stresses.

In the construction shown in Figure 1, the thermal expansions of the component and the printed board can be assumed to be different, and the thermal mismatch Du is given by:

$$\Delta u = \Delta e \times L \times \Delta T$$

where

De = the difference in CTE between the materials

L = the longest dimension of the component (often the diagonal)

DT = the temperature change

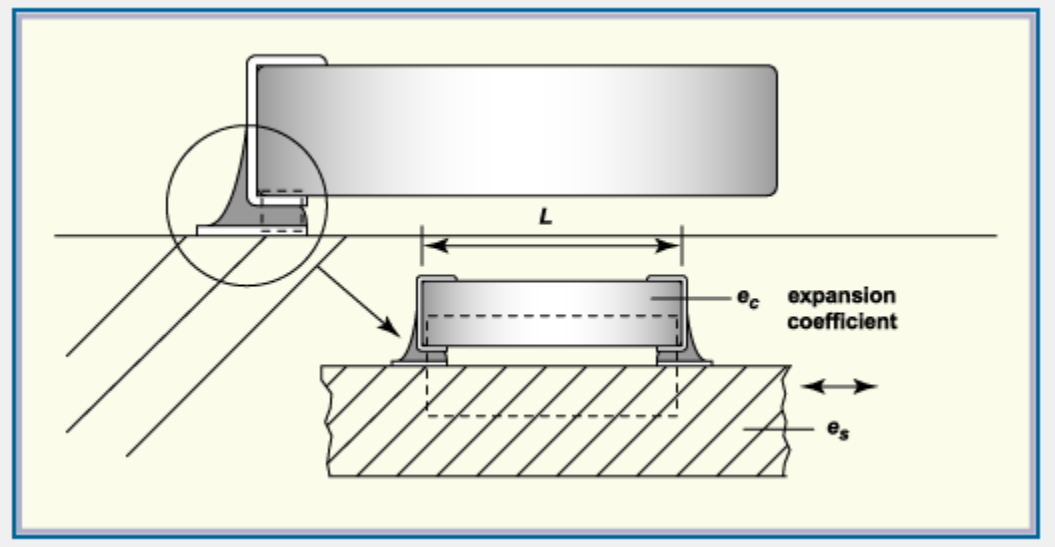


Figure 1: Thermal mismatch in solder joints

In most mechanical structures, such thermal mismatch would be accommodated by elastic deformation, resulting sometimes in a high stress in the structure. With

soldered assemblies, however, the situation is different, as the strength of the solder is low compared with that of the usual engineering materials. With leadless components, the materials of component and substrate are comparatively so rigid that a large part of the mismatch has to be accommodated by plastic deformation in the solder joints. In this case, repeated movement due to temperature changes produces a cyclic stress (Figure 2), and fatigue failure may eventually follow.

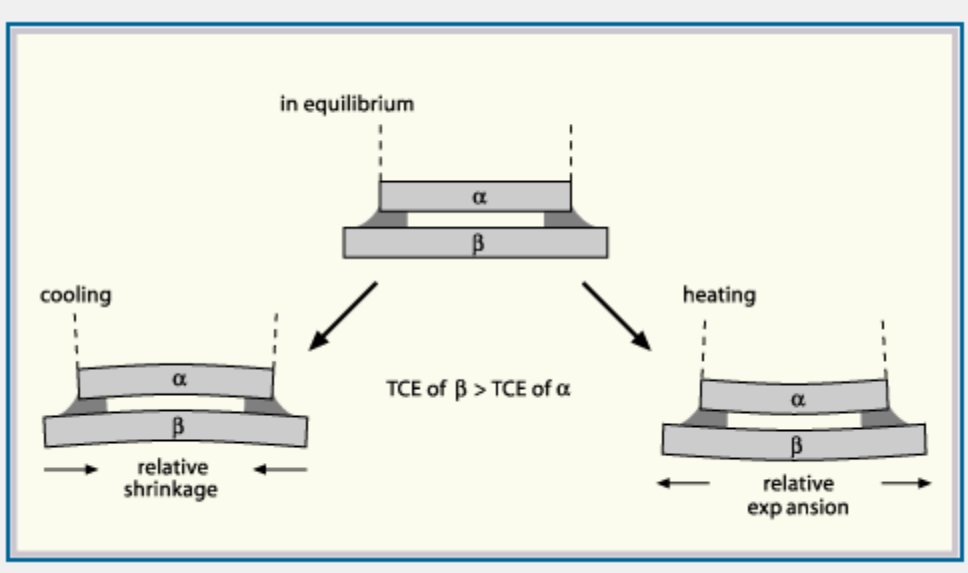


Figure 2: CTE mismatch producing cyclic stress

The shear strain experienced depends on the CTE mismatch between the materials and the length : height ratio of the joint. As CTE mismatch increases, so does the strain, and thus the thermal cycling life decreases. If rigid solder joints are to survive cycling during the specified life, the component size may have to be limited or the stand-off height increased to withstand large temperature fluctuations and CTE mismatch. The Column Grid Array is an example of a package where the stand-off height is deliberately made higher than a normal BGA (by using columns of high-melting solder) in order to accommodate CTE differences between its ceramic body and a PCB substrate.

Column grid array detail

Thermal mismatch, as a cause of plastic deformation in the solder, leading to fatigue fracture, finds its origin not only in differences in CTE, but also in differing rates of temperature change. During both soldering and operational life, the rates of heating and cooling of components and substrate are in general not the same, so that temperature differences are created, even if the CTEs are matched, and these temperature differences generate stresses. In practice, the stresses fortunately remain fairly small, provided that no incorrect constructions have been used. However, if the rate of temperature change is very fast, as is the case in thermal shock testing, these stresses may become high.

So far we have been looking at rigid joints. However, with components having relatively flexible leads, a considerable part of the mismatch can be taken up as elastic deformation. But what kinds of joints are present on an assembly? And how well are they likely to stand up to thermal fatigue?

Rigid joints

The rigid lap joint occurs in a number of forms within printed circuit assemblies. It occurs on leadless chip components (Figure 3) such as chip capacitors.

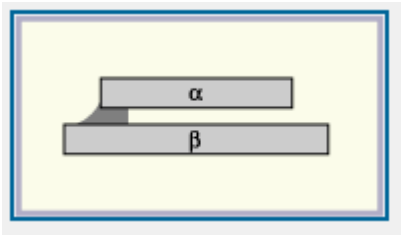
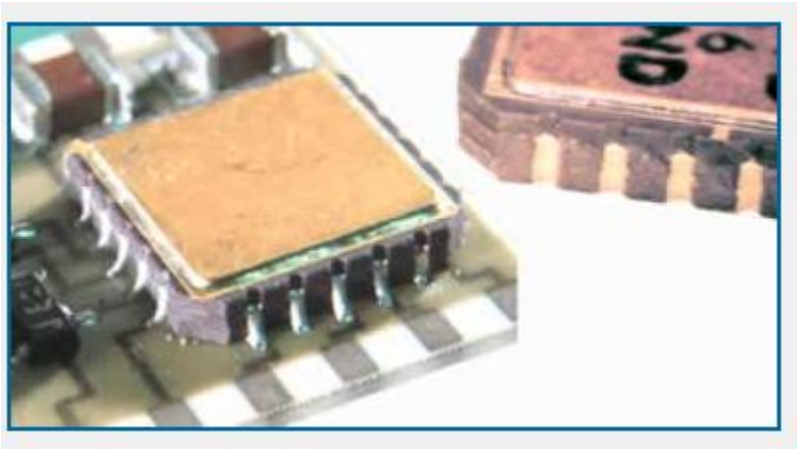


Figure 3: A cross-section through solder structure – leadless chip

This is one of the larger and stronger joints in the surface mount family because of the outside fillet. However, the conceptually similar joints on leadless chip carriers are by far the most troublesome type of joint, because the components are large and joints are relatively small and weak. For this reason, leadless chip carriers often have extra solder areas on the side of the carrier. Usually semicircular, these are referred to as 'castellations'. However, it is still not proven whether such side joints improve long-term reliability, and non-uniform joints on the periphery of a carrier tend to cause stress concentration, leading to the failure of individual fillets.



Castellations on a leadless chip carrier

Die/substrate and similar bonds (Figure 4) also use a lap joint, and here the limitation in component size is most evident. Where a continuous thin joint is not required (for example, for thermal reasons), then one strategy to reduce stresses is to divide the bond area into a number of discrete pads using 'solder dams'.

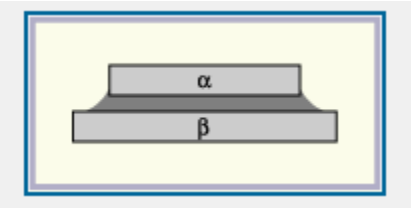


Figure 4: A cross-section through solder structure – die or substrate bonding

Solder bumps (Figure 5), as used in the ball grid array or flip chip, represent a form of multiple lap joint in which the size of the joint elements has been defined in this way, usually by solder resist.

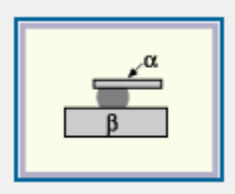


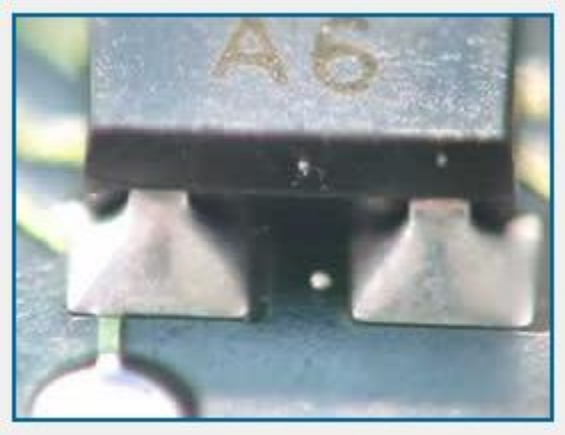
Figure 5: A cross-section through solder structure – solder bump

All forms of lap joint share the basic problem that any mismatches of CTE must be accommodated by the joint. This limits the size of the parts being joined, and joint reliability depends on:

- the linear dimensions of the joint
- the solder joint thickness
- the mechanical properties of all the materials used.

Compliant joints

The compliant lap joint used with leaded components (Figure 6) is generally smaller than the rigid lap joint, and lead flexibility is intended to compensate for any CTE mismatches. However, lead compliance is a major factor in determining stress on the joint, and this depends on the design: there can be a >100:1 variation in joint stiffness. More seriously, if the amount of solder is excessive or uneven, this counteracts the intended flexibility of the lead.



Excessive solder reduces lead compliance

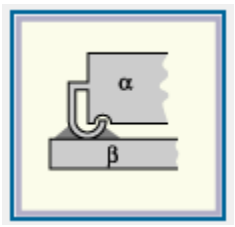


Figure 6: A cross-section through solder structure – compliant leaded chip carrier (J-lead)

Any expansion due to CTE mismatches will cause stress concentrations at the heel of the joint, where failure normally starts. The strength of the minimum-solder joint thus depends on the quality of the heel: while the fillet should not rise more than two-thirds of the height to the knee, it must be above the heel.

The compliant butt joint (Figure 7) is used with leaded components like plastic leaded chip carriers (PLCCs), where the lead is usually bent into a 'J' shape. This narrow solder fillet is very attractive for high density designs and again relies on lead geometry and flexibility to compensate for any mismatches in CTE. However, this is inherently a weak fillet, and it cannot be strengthened by placing solder on top of the lead, inside the curvature.

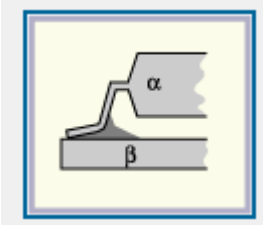


Figure 7: A cross-section through solder structure – compliant leaded chip carrier (gull wing)

The attachment reliability is determined by:

- the diagonal lead stiffness
- the minimum load bearing area of the joint which is subjected to a shear force transmitted by the lead
- the solder joint thickness.

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