ELECTRONICS MANUFACTURE-The In-Circuit Test sequence

In-Circuit Test comprises several sections, each consisting of a series of tests on individual devices. By testing devices individually, failures can be determined at the device level, and diagnostics are simplified. The arrangement of the sections grants devices maximum protection from damage due to manufacturing defects. The sections are listed below in order of execution.

Pre-shorts

Pre-shorts testing allows the test operator to bring the board under test to a known state before the shorts test is run. The operator is prompted to set potentiometers, switches, and jumpers on the board. After all operator actions are complete, the board is ready for the shorts test.

Shorts and opens

These are the equivalent tests to the continuity and insulation resistance tests described above for bare boards. The shorts and opens testing detects unexpected opens and shorts on the board under test. If any are detected, the board fails and no further testing takes place.

The opens test verifies that all expected shorts are present on the board, for example, jumpers and inductors. A resistance measurement is made between a pair of nodes that are expected to be shorted. If the resistance is less than or equal to a threshold value (a short), the test passes. If the resistance is greater than the threshold (an open), the test fails.

The shorts test detects unwanted shorts. The shorts test consists of two phases: a detection phase and an isolation phase. During the detection phase, each node is tested for unexpected continuity to all other nodes. If a measured resistance is less than or equal to a defined threshold (a short), the isolation phase is executed to determine which of the nodes under consideration is shorted to the node being tested. Shorts and opens thresholds are determined from the circuit description and are set individually for each node.

Unpowered analogue

Unpowered analogue testing verifies the values of individual components on the board under test. The tests are performed with the board in an unpowered state. Each Unpowered analogue test can fit into one of two general categories:

Constant AC/DC voltage test – A known voltage is applied across the component under test and the resulting current flow through the device is measured. This method is used for testing passive, linear components such as resistors, capacitors, and inductors.

Constant current test – A known current is applied through the component under test and the resulting voltage across the device is measured. This method is used for testing passive, non-linear components such as conventional diodes, Zener diodes, and transistor PN junctions.

Eliminating the effect of parallel impedances is a crucial part of unpowered analogue testing. Direct and indirect parallel impedances from other components on the board tend to introduce a significant error. A method known as guarding may be used to eliminate some of the parallel impedances. However, not all parallel impedance paths can be eliminated in all situations.

Unpowered vectorless

Unpowered vectorless testing is designed to locate device pins that are not properly soldered to the board and polarised capacitors that have been installed with the wrong orientation. These tests are performed without power to the board.

Unpowered vectorless testing is typically used to test SMT connectors, complex devices without test patterns, and complex devices requiring a short test lead-time. This technique can also verify the orientation of polarised capacitors whereas the standard analogue measurement cannot. The ability to accurately detect capacitor polarity relies heavily on the size, package and physical orientation of the capacitor. Tantalum and aluminium surface mount capacitors or axial lead capacitors can be checked for polarity orientation as long as a plate can be mounted over the top of the capacitor. Large value capacitors and capacitors in parallel with many other capacitors may not be testable using this technique, but the value of the capacitor can still be checked during unpowered analogue testing.

Capacitively coupled

A plate mounted in parallel to the device under test (DUT) is placed so that it is as close to the device as possible. An AC source is applied to the individual pins of the device that creates an electromagnetic field between the device pins and the plate. Field strength is measured as a voltage and if the received voltage is greater than or equal to the specified threshold, the pin passes. If the voltage is less than the specified threshold, the pin will fail. This test simply verifies continuity between the DUT and the PCB. If more than one pin of a device is connected to the same net, this testing technique does not verify that all the pins are making contact with the net. It only verifies that at least a single pin is connected to the net. For this

reason, multiple ground and power pins on a single device package cannot all be tested individually for continuity to power and ground.

Diode drop

Ground pins cannot be tested using this technique. All other pins are tested for a diode drop to ground. The pins are tested by applying an AC source at different thresholds and frequencies and reading the resulting voltages on other pins of the device (detector pins). The detector pins may be DC biased to allow a stronger signal to propagate through the device. The test limits are learned using a software algorithm and a known-good sample board. Test coverage using this technique can only be assessed after the test program is in place.

Controlled power-up

Once the pre-shorts, shorts and opens, unpowered analogue, and unpowered vectorless tests have been completed, the controlled power-up test is performed. Power is applied to the board at the specified voltages while supply currents are closely monitored. If the board draws more current than the board specification allows, the power supplies are immediately shut down and the test fails. The intent is to avoid damage to the components on the board from defects not found during previous tests. Such defects include reversed polarity of electrolytic or tantalum capacitors, incorrect orientation of integrated circuits, and other similar problems.

Digital

Digital testing attempts to isolate and test each digital device individually. This allows for maximum diagnostic capabilities with minimum customisation of tests for different boards.

These tests are designed to verify that the correct device is loaded on the board, is oriented and functioning correctly, and has all pins properly soldered. Inputs are supplied to each device using drivers that have adjustable voltage and timing settings. Outputs of the DUT are connected to programmable receivers and are verified against expected results. Less complicated devices are usually fully tested and all internal logic functions are exercised. However, complex devices, such as microprocessors, are fully tested for pin function, but not for full logic function.

To isolate digital devices, all the surrounding devices are disabled. Disabling is the process of placing the device pins on a particular node into a high-impedance state - except for the pins of the particular device being tested. When this is accomplished, the tester has the ability to drive and receive on a node without contention from other devices. In cases where it isn’t possible to disable all the other devices on a node, the outputs on the surrounding devices connected to inputs on the DUT must be back-driven.

Powered analogue

Analogue devices like op amps, voltage regulators and oscillators are tested with power applied to the board. AC and DC voltage sources are used to stimulate the device, and AC and DC detectors are used to verify the response of the device.

As with digital testing, analogue devices must be isolated by disabling other connected devices. Disabling allows stable, repeatable analogue measurements to be taken on the DUT. When disabling methods are not available, back-driving may be used to overcome device contention. Back-driving is not recommended as an alternative to placing device pins into a high-impedance state because of the risk of device damage.

Digital and analogue mixed

Devices such as analogue to digital converters and digital to analogue converters require a mixed test method. In mixed testing, digital drivers and receivers are used on the digital pins of the device and analogue sources and detectors are used on the analogue pins.

Disabling devices connected to the DUT is very important for mixed testing, as the time required to set up and run a mixed test is typically much greater than for digital or powered analogue tests.

Vectorless test

An option on some equipment is what is referred to as ‘vectorless test’. The term means that no ‘test vectors’ are required: in other words there is no need to develop test patterns, or sets of test inputs which are applied to the product in order to identify faults and distinguish correct systems behaviour from incorrect. This is particularly helpful in the case of mixed signal circuits, where automatic generation of test vectors is less well established than for digital integrated circuits.

One vectorless test strategy is indicated in Figure 5. The sequence involves making contact to pairs of pins, and the sequence is:

Apply voltage to pin A and measure current

Apply voltage to pin B

Re-measure current flowing through pin A. If both pins are connected properly there will be a change in the current. No change in the current indicates a pin fault.

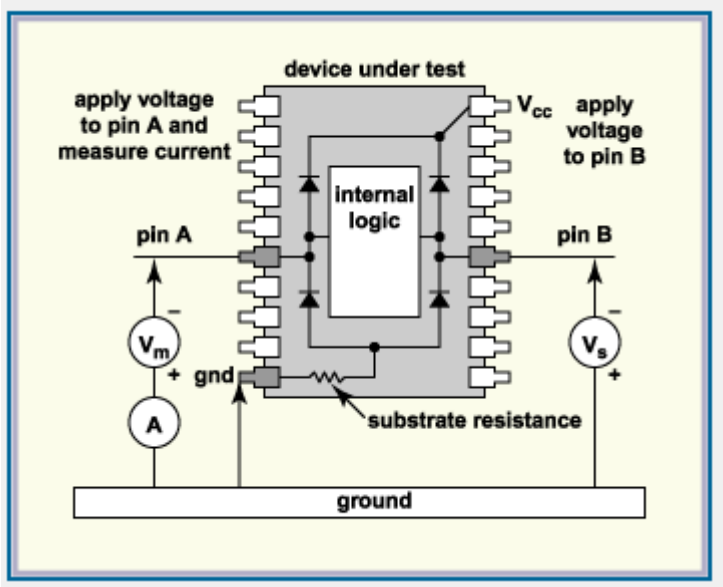

Figure 1: Vectorless testing

Vectorless testing

Whilst no information on the function of the device under test is required, pin assignations are still needed. However, this information is available from the CAD system. The greater advantage from the manufacturing point of view is that, like ICT for passives, the problem is traceable to specific pins, and therefore much easier to deal with.

So far, we have implicitly assumed test solutions which have a test driver/receiver channel on every pin, or the equivalent provided by some method of multiplexing. Vectorless tests are also available using inductive or capacitive probes to stimulate the package. Again, less device specific information is needed than would be the case for a full exercising of the device under test.

Powered functional

Situations arise where it is advantageous to test a portion of the board as a functional cluster. A functional cluster is a group of components that are configured to perform a definable and testable function. Examples include analogue filters and amplifier circuits.

Functional testing may also be necessary due to a lack of full nodal access to the board. In this case, accessible inputs are stimulated, and circuit response is verified on accessible outputs.

The disadvantage of powered functional testing is the loss of diagnostic capability. If a functional block fails, it isn't possible to accurately determine which particular device caused the failure.

The greatest advantage of powered functional testing is in using it as an addition to a full in-circuit test. The advantage of device level diagnostics is retained while also verifying that groups of components work together as designed.

Board level functional

Some kinds of board level functional tests can be run on the ICT. These differ from powered functional tests in that a dual-level fixture is used to disconnect the board from probes used for ICT. Only probes used for the functional tests remain in contact with the board, thus reducing noise and loading.

Board level functional test relies on instruments within the ICT along with external instruments such as oscilloscopes, frequency counters, high-voltage supplies, and RF sources. A detailed functional test specification is required and not all functional test requirements are possible on the in-circuit tester.

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