ELECTRONICS MANUFACTURE-Common processes-Underfilling

In an area array, especially with small structures as in CSPs or flip-chips, TCE mismatch between die and substrate places strain on the solder joints, which can result in fatigue failure of the joint during thermal cycling. The strain is proportional to the distance from the 'neutral point' at the centre of the chip, so that joints furthest from the centre are most susceptible to failure, and increasing the size of the chip increases the stress experienced.

There are two ways of reducing the level of strain:

- by increasing the column height
- by locking the die and substrate surfaces in place with an underfill resin.

It has been observed experimentally that increasing the solder volume, resulting in an increased gap height, improves thermal shock performance, and that early thermal shock failures can be induced by having insufficient solder at the bond pad site.

Both analysis and experiment confirm that the reliability of the assembly can be enhanced by introducing an encapsulant between chip and substrate. This couples silicon and substrate and locally constrains the TCE mismatch, reducing the strain on the flip-chip. Also, by completely filling the space between die and substrate, the area which is stressed becomes the entire die area instead of just the total area of the solder bump cross sections.

The resin is dispensed in a line along one or two edges of the die and allowed to seep under the die by capillary action. The substrate is heated (typically to around 70ºC) to enhance capillary flow, but the time for underfill to be complete may be as much as 15 minutes, depending on the size of the die. The dispense cycle and line geometry is optimised to allow complete underfill and make a fillet of uniform radius around the complete die perimeter. The encapsulant provides not only mechanical and thermal coupling between die and board, but also forms a protective barrier layer on the active face of the IC chip.

Care has to be taken to avoid contamination which would block the needle or bubbles of air which might become trapped under the die, because large voids in the underfill affect reliability. Where a void totally surrounds a solder joint, that unsupported joint will fail earlier than an encapsulated one, due to fatigue. There may also be what are referred to as 'pitted voids' in the area of the solder joints, which are formed by the shadowing effect of the joint on the encapsulant flow.

Sometimes solder is extruded into the void, but there is no evidence that this mechanism or these voids cause unacceptable changes in performance.

Most encapsulants used are silica filled epoxy based materials, with anhydride based curing systems, requiring cures of 1 hour at temperatures of 130–150ºC. Epoxies for this application are supplied premixed and frozen, and have very low levels of ionic contaminants, but are thinner than normal encapsulation compounds, and contain fillers with smaller particles. These fillers modify the TCE of the epoxy to match substrate and die, so that the epoxy does not add to thermal stress.

Filler particles cause difficulty when dispensed under a flip-chip, because filling the gap requires capillary action. Arnold pointed out that the resin and filler have different densities and flow characteristics, so that laminar flow cannot occur with a filled material. Whilst pre heating filled encapsulants may increase the flow rate of the organic portion, this also reduces the ability of the resin to move fillers through the gap. In theory the result could be uneven distribution under the chip, causing thermal stress because of the TCE imbalance. In practice, Baggerman reported that, with a chip to polyimide gap of only 55µm so that filler particles were excluded, no failures were observed after 2,000 thermal cycles. Perhaps the most important factor is that the whole of the volume should be filled with resin. However, a real disadvantage of a rigid epoxy underfill is that it is sensitive to gross distortion of the substrate.

Arnold suggests the use of aerobic urethane underfills, which combine high adhesive tensile strength with high elongation. A soft and flexible urethane backbone acts as a shock absorber, effectively dissipating both mechanical and thermal shocks. In contrast, a brittle epoxy can be more rigid than solder or bond wires and would transfer stresses to these parts of the assembly.

Arguably there may be a real choice between using materials with high adhesion and low modulus, and selecting more rigid materials, provided that these are adequately matched. Goldstein found that, when subjecting underfilled samples to 1,000 thermal cycles, the change in measured characteristics was lowest for the samples underfilled with resin having a TCE most similar to that of the solder. O'Malley suggests that it is the underfill chemistry which is critical, as it affects the adhesion of the encapsulant to the chip surface. Experiments must be carried out to verify the choices made.

When an underfilled flip-chip assembly is tested to destruction by thermal cycling, the dominant failure mode is delamination of the interface between the active face of the die and the underfill. Once adhesion between these surfaces is lost, the flip-chip joints are directly subjected to the strain resulting from the thermal mismatch between die and board. Electrical failure follows shortly after delamination as the result of solder fatigue cracking.

The number of thermal cycles required to initiate failure can vary greatly, depending on the materials used and the process parameters, but flip-chip assemblies routinely survive 2,000 cycles from −40ºC to +120ºC with no failures. In fact, flip-chips have been claimed to be more reliable than conventionally packaged devices, reputedly due to freedom from gold aluminium intermetallic growth catalysed by trace quantities of halides in the packaging.

Author: Martin Tarr

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