Electronic materials and components-Semiconductor packages

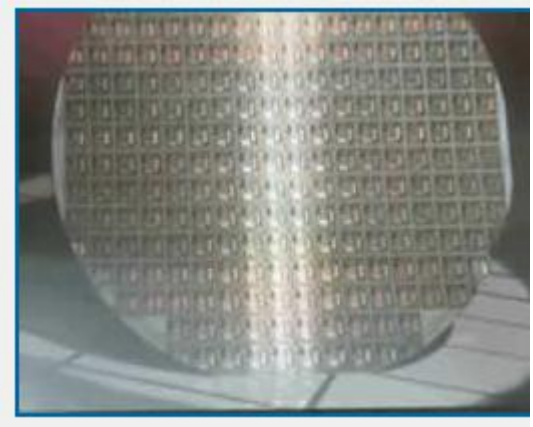
Semiconductor 'back-end' processes

We will learn much more about semiconductor 'back end' processes in subsequent modules, but you need to understand at least something of the terminology and what is involved in turning a 'chip' into a finished package1.

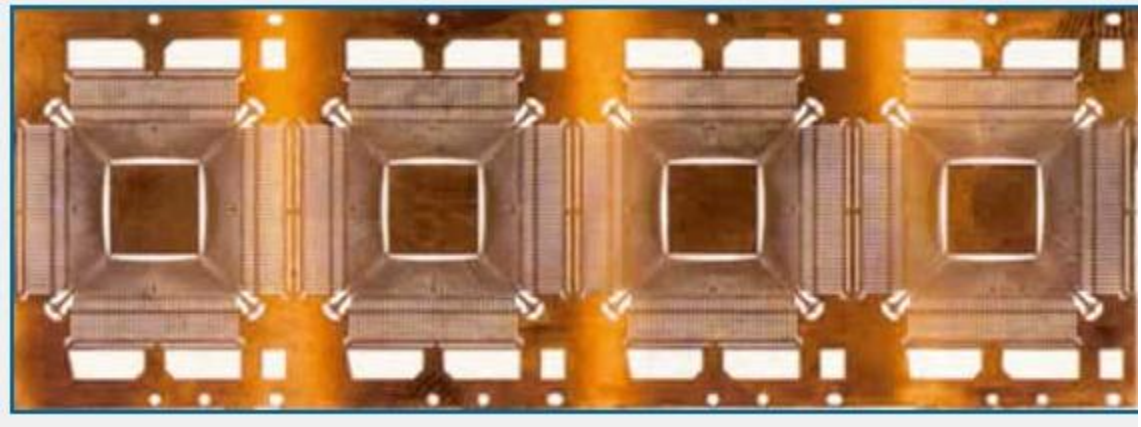
1 It is always very dangerous to point people at sources of information on packaging, especially now that the wonderful Fullman site has disappeared. However, you might like to take a look at what a doctoral student can achieve at http://chenjian.virtualave.net/packaging.

The starting point for semiconductors is the wafer, which contains a (very large) number of devices, separated by small gaps, and electrically isolated from each other as part of the processing. Starting with a blank wafer of extremely pure silicon, building up layers by deposition techniques, etching patterns, and implanting dopants into the silicon structure using high energy particles, the semiconductor 'fab' ships a wafer which is partially probe-tested, but needs terminations in order to communicate with the outside world. These 'front end' processes attract the headlines, but the back end of the pantomime horse is just as important!

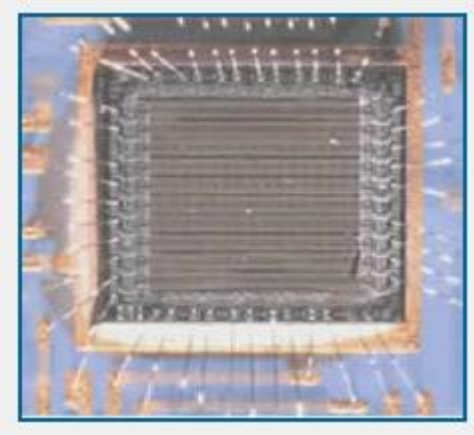
The 'back end' process consists of sawing the wafer into individual dice (the terms 'chip' and 'die' are equivalent), mounting the die on a lead-frame or other mount using conductive adhesive, and finally making fine wire connections to the top surface – this 'wire bonding' process uses gold and aluminium wires typically 25-33 μm in diameter. Because wires and semiconductor are relatively fragile and easy to contaminate, the die will then be protected in some way.



A silicon wafer



Lead-frame for a 128-pin QFP



Silicon die wire-bonded onto a ceramic substrate

The first solid state devices were incorporated into high reliability military and telecommunications applications, and needed a hermetic package to prevent junction leakage and degradation of transistor gain caused by moisture and contamination.

Packages were made either of metal, with glass-to-metal seals isolating the leads, or of ceramic: both technologies were expensive, and often relatively large and mechanically fragile. However development of silicon planar technology, improvements in methods of passivation for the die surface, and advances in polymer formulation and purity, combined to make it possible to mount a silicon die on a free-standing lead-frame, encapsulate the assembly in resin (usually by transfer-moulding), and create a protected device reliable enough for most applications.

Discrete semiconductors

Transistors and diodes

Discrete transistors and diodes are generally available in standard Small Outline Transistor (SOT) packages originally designed for use in hybrid microelectronics assembly. Although there are moves to introduce smaller variants, the most common of these is the SOT-23 (now renamed in the American JEDEC standard as TO-236). The construction of a typical SOT-23 package is shown in Figure 1. The SOT-23 can accommodate almost any semiconductor with a die size up to about 0.75 mm square, and its power handling capabilities make it suitable for small-signal transistors.

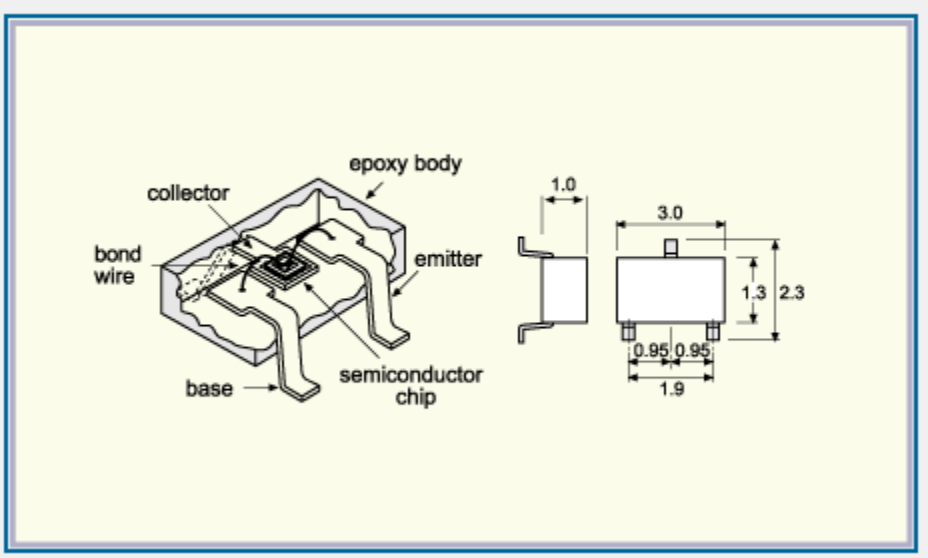
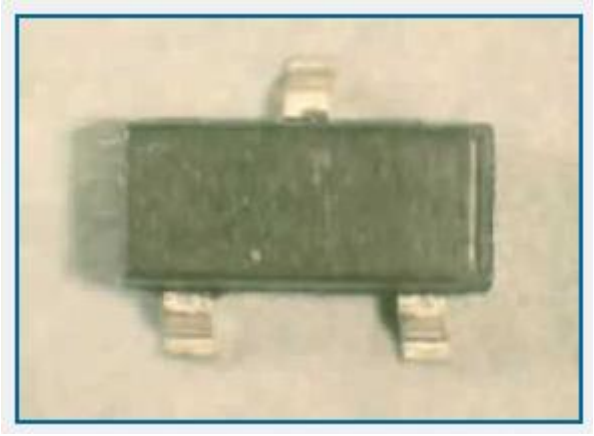


Figure 1: Construction of the SOT-23 package



[SOT-23 (Small Outline Transistor or Diode) package]

There have been many criticisms of the design, which was an early-1970s compromise, and comparatively large. Improved internal constructions have made

it possible to develop a range of more compact devices, which are more compatible with the smaller multi-layer ceramic capacitors now in common use. The smallest of these currently has a moulding size of 1.6 × 0.8 mm, with a seated height of 0.7 mm, and lead centres on 1.0 mm pitch, occupying only 30% of the mounting area of a standard SOT-23.

There are a number of similar packages, differing in their size, power handling capacity and number of leads, but using the same basic concept. In all cases the trend is towards smaller packages, and finer lead pitches.

Dissipating more heat generally demands a heavier metal leadframe. As an example, semiconductors on chips up to about 1.5 mm square can be packaged in the SOT-89 format, shown schematically in Figure 2. Its three leads are all along the same edge of the package but the centre one extends across the bottom to improve the thermal conductivity. Whilst the SOT-23 can dissipate typically 200 mW in free air at 25°C, the SOT-89 can handle up to 500 mW under the same conditions.

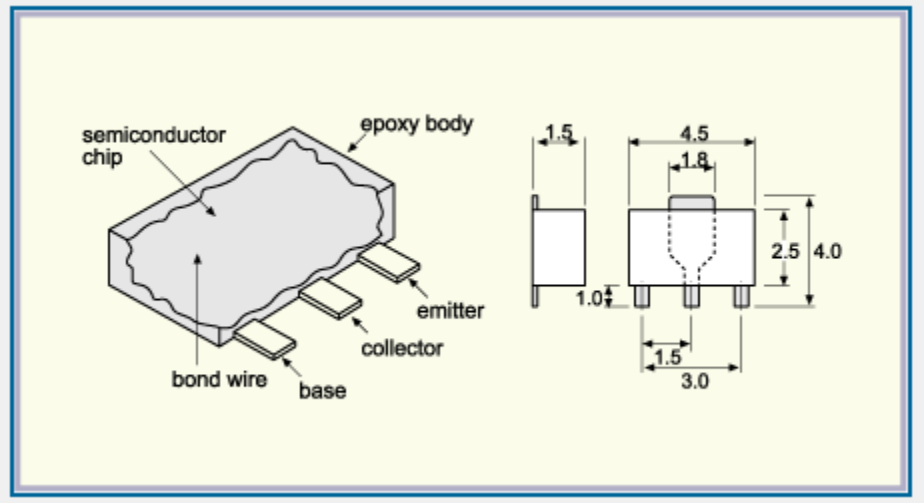
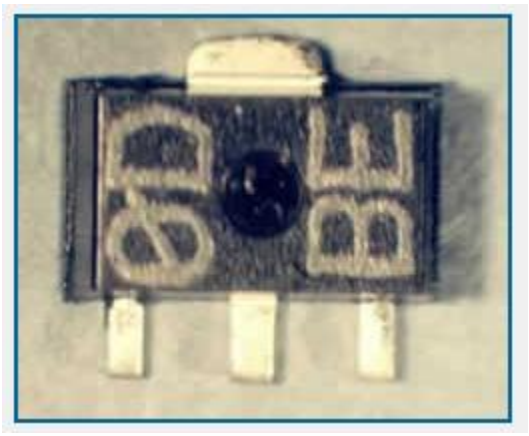
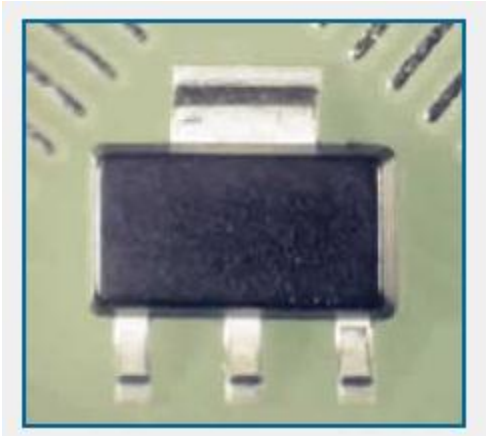


Figure 2: Design of the SOT-89 package



[SOT-89 package (for increased dissipation)]



SOT-223 package (updated SOT-89)

Diode formats

Discrete diodes are frequently packaged in SOT-23 format: one of the three contacts may be redundant, although diode pairs with either anodes or cathodes connected together are common.

However, several two-terminal hermetically sealed glass-to-metal packages have been developed especially for diodes, the two most popular both being cylindrical. The MELF is so-called because its appearance and dimensions (Figure 3) are similar to those of the earlier MELF (metal electrode face bonded) resistors. With adequate cooling, power dissipation can be as high as 2 W.

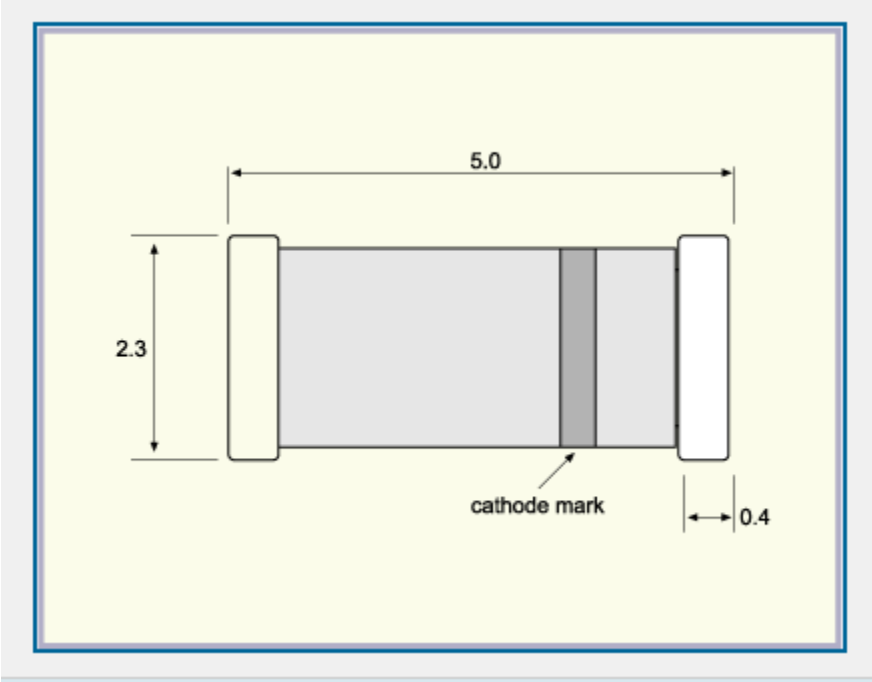


Figure 3: MELF diode

MELF (Metal Electrode Face Bonded) diode

The SOD-80 ('Small Outline Diode') encapsulation (or 'MiniMELF') is 3.6 mm long and 1.6 mm in diameter. It is cheaper, lighter, and requires less board space than the SOT-23, but has no flat top surface and can be more difficult to handle. Its construction is specifically designed for small diode chips and the package dissipation is limited to 250 mW.

Cylindrical packages have no flat top surface and are sometimes difficult to handle. The manufacturing costs of glass parts may also be higher than for plastic encapsulations. For these reasons, moulded plastic packages such as the DO-214 (Figure 4) are becoming increasingly common. Different sizes of package, with

more or less heat sinking, are selected according to the die size and current/power rating of the application.

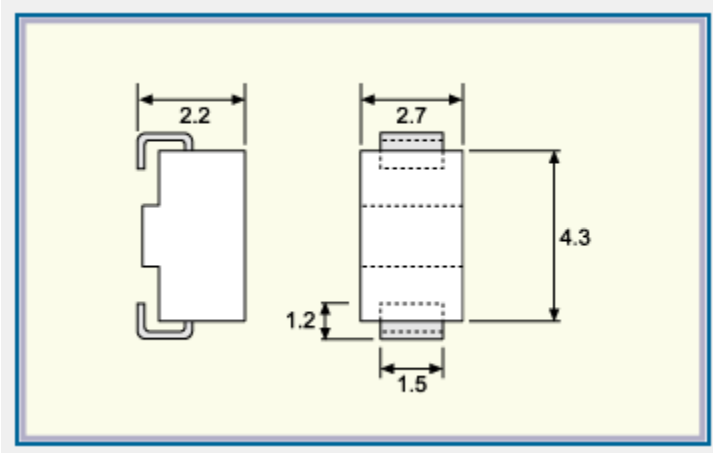
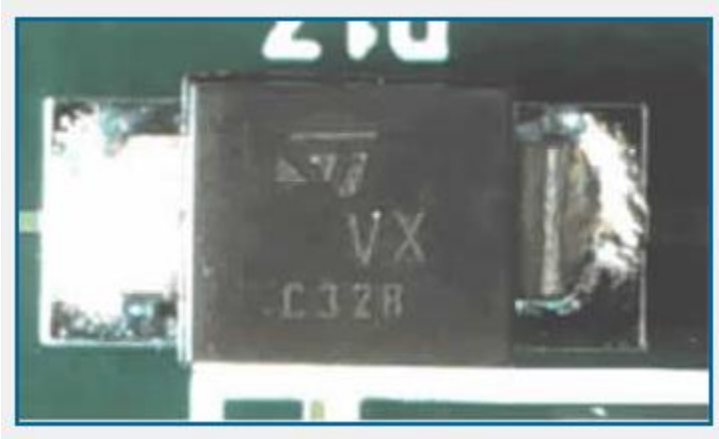


Figure 4: Typical dimensions of DO-214 package



Moulded plastic diode package

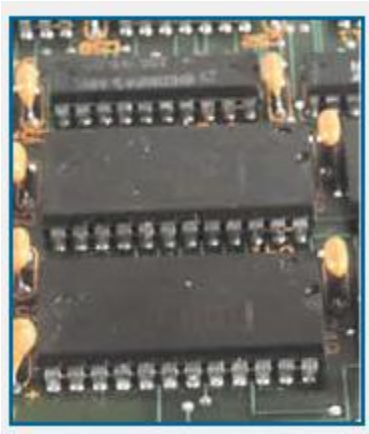
Although originally applied to resistors, and to diodes in glass encapsulation, the end cap concept is also seen applied to square bodies for other types of component.

Power devices

As you will have deduced from the different Small Outline packages for transistors, higher power means that more heat energy has to be removed from the package, and this usually means the incorporation of a larger metal structure in order to conduct heat from the die where it is dissipated.

Full consideration of this topic is beyond the scope of this module, but you should be aware that, in power devices, adaptations have to be made to the ways in which bonds are made to the die reverse and to the top surface. Typically requirements for external heat sinking must be observed in order to prevent the component 'burning out'. Power devices are also generally associated with higher-than-average currents, and this aspect is one more factor to be considered during board design.

Integrated circuits



Dual-in-line packages

The dual-in-line package (DIL or DIP) has a number of disadvantages which began to become apparent as the pressure increased for higher lead-count devices:

A DIP with large numbers of pins in a double row at a (0.1 inch) pitch becomes relatively expensive because of excessive size and material use

The DIP format results in long internal lead lengths for the pins towards the ends of the package, with consequent higher inductance and inter-lead capacitance, limiting device performance

The package occupies more board area than is necessary, since board manufacturing technology has advanced to accommodate much smaller lead pitches. Figure 5 shows a typical design plan of a 64-pin DIP and demonstrates how inefficient is its use of board area

Larger sizes of DIP become progressively difficult to handle robotically and to insert automatically into plated through-holes.

In short, it is the mechanical properties of the package that have physically limited the size to which the DIP can grow.

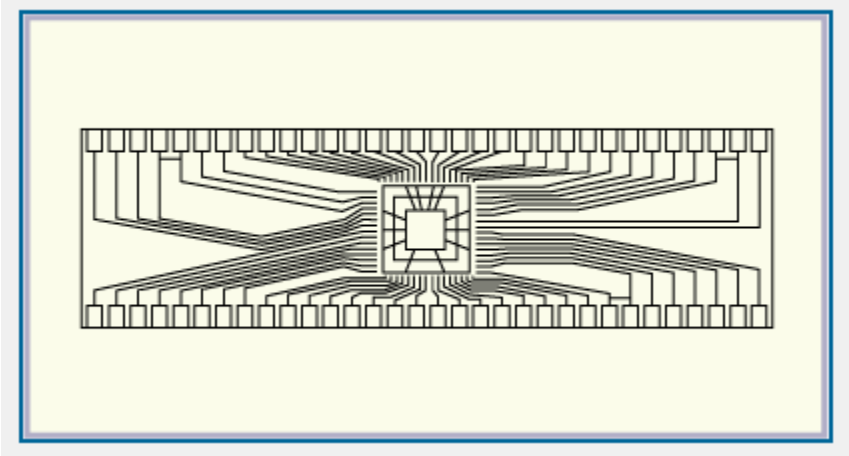


Figure 5: Schematic of a typical 64-pin DIP lead-out pattern

As the technology of surface mounting has developed, a range of packaging types has therefore emerged, some by transposition from the hybrid microelectronics industry and some by development in their own right.

Leaded IC packages

The small outline transistor (SOT) and the small outline integrated circuit (SOIC, or simply SO) packages have a longer history of use than other surface mounting devices. The SO package was developed in Europe in the mid-1970s particularly for the emerging electronic watch market.

The SOIC is a plastic package, available in 6, 8, 10, 14, and 16 pin versions with a body width of 4 mm, and in 16, 20, 24 and 28 pin versions with a wider body of 7.6 mm. The flattened leads are on standard 1.27 mm (0.05 inch) centres and are formed outwards in a ‘gull wing’ fashion, so that the tips of the leads lie in contact with the PCB. The package outline and typical dimensions of the SOIC range are given in Figure 6 and Table 7. They may vary very slightly from one manufacturer to another except for the lead pitch which must be 1.27 mm.

QFP gull wing terminations

The low lead-count SOICs require less than half the area of their DIP equivalents and weigh only one-tenth as much.

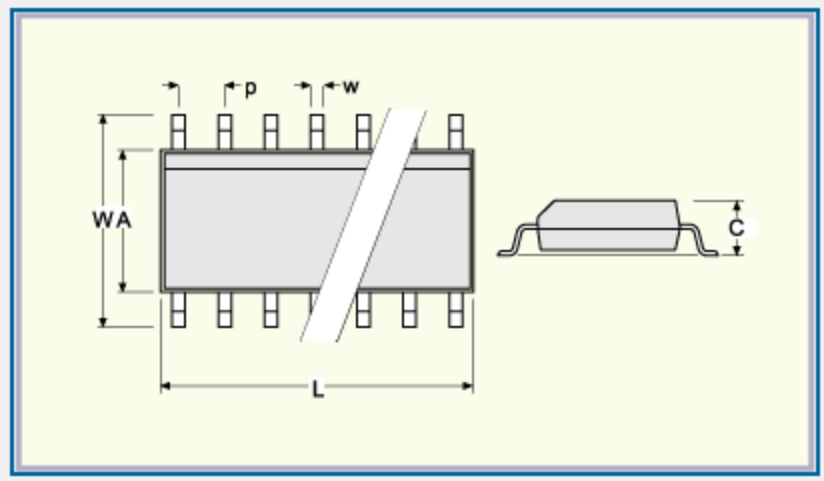
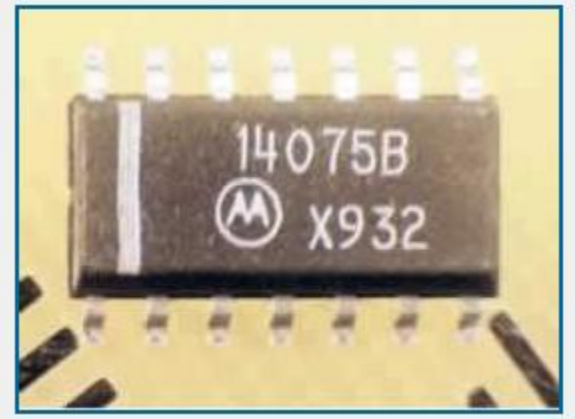


Figure 6: Design of the SOIC range of packages



SOIC-14 (Small Outline Integrated Circuit)

Table 7: Dimensions of SOIC packages

Type	Leads	Pitch mm (p)	Width mm (w)	Length mm (L)	Body width mm (A)	Device width mm (W)	Height mm (C)
SO-6	6	1.27	0.4	3.75	4.0	6.2	1.6
SO-8	8	1.27	0.4	5.00	4.0	6.2	1.6
SO-10	10	1.27	0.4	6.25	4.0	6.2	1.6
SO-14	14	1.27	0.4	8.75	4.0	6.2	1.6
SO-16	16	1.27	0.4	10.00	4.0	6.2	1.6
SO-16L	16	1.27	0.5	10.50	7.6	10.65	2.6
SO-20	20	1.27	0.5	13.00	7.6	10.65	2.6
SO-24	24	1.27	0.5	15.60	7.6	10.65	2.6
SO-28	28	1.27	0.5	18.10	7.6	10.65	2.6

SOIC-20

The SOP concept has more recently been extended to include a wide range of thinner, smaller packages, many with smaller pitch centres.

Quad flatpacks

The basic construction of the SO package is also seen in the Quad Flat-Pack (QFP), which has leads on all four sides (Figure 7). The leads are also formed to a ‘gull-wing’ profile to bring their ends level with the bottom of the package, but in this case there are many variants: some devices have very flat profiles, whilst other styles are much deeper. As with the SOP, the QFP trend has been towards thinner packages, with more and finer leads: computers typically use components with 200–250 leads on 0.4 mm or 0.5 mm pitch.

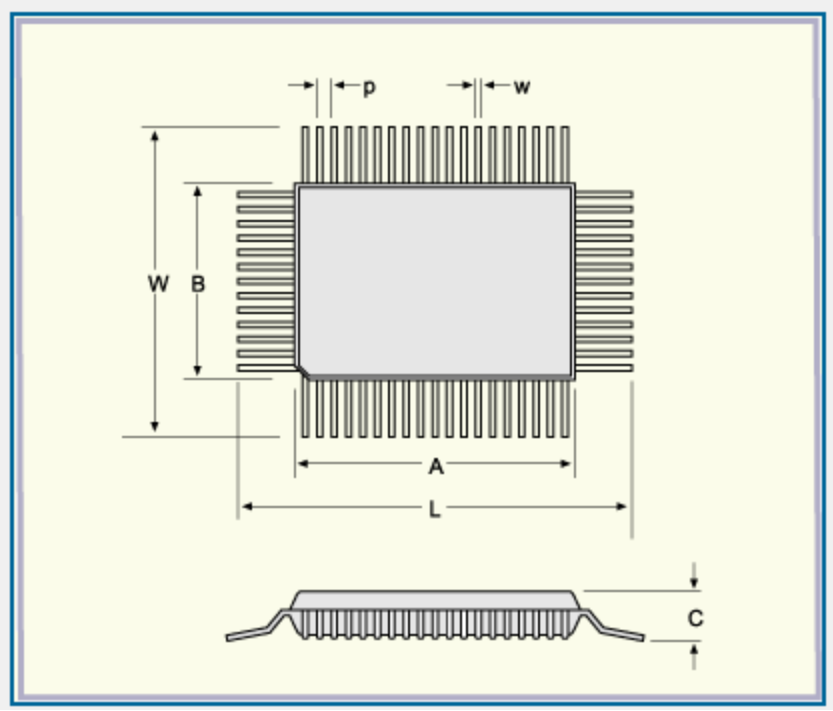
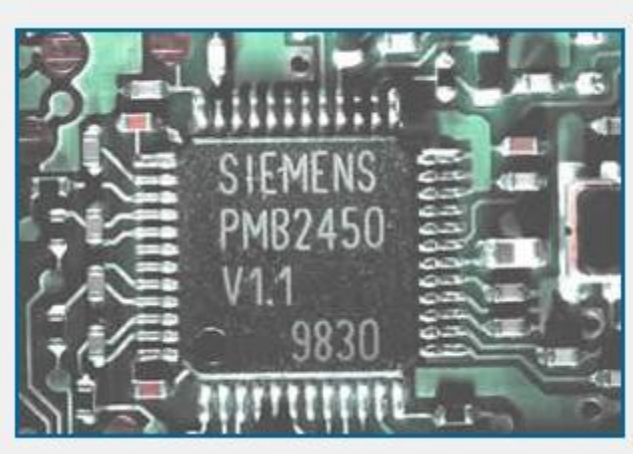


Figure 7: Views of a gull wing Quad Flat Pack



[Quad flat package (1.27mm pitch leads)]

Pitch spacings down to 0.4 mm (0.016 in) allow pin counts of over 200. Typical examples have 44 to 150 leads with body sizes up to 25.4 mm square and lead pitches of 0.5 to 0.8 mm.

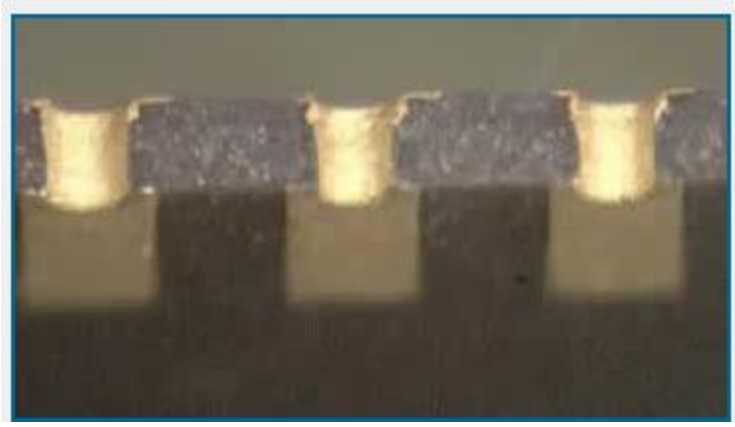
Trend towards QFPs with finer pitch leads

At high lead counts, the gull-wing leads are very thin and narrow, and therefore in danger of being deformed during handling. This puts a constraint on both placement machines and operators to avoid such damage.

The chip carrier concept

The term ‘chip carrier’ refers to a range of IC packages that are square or rectangular, with terminations brought out on all four sides. The first of these to be developed was the leadless ceramic chip carrier (LCCC). This can be envisaged as the useful active centre of a hermetic DIP, with all the leads and excess packaging material discarded. Since it is constructed of the same materials and in the same manner as hermetic DIPs, it is at least as reliable. Leadless ceramic chip carriers were commonly available in sizes from 5 mm square to 25 mm square and above, with 1.27 mm (0.050 in) lead pitch, and from 20 leads to upwards of 100.

Leadless ceramic chip carriers are constructed in a variety of ways that are dictated by the end product use and the cost of manufacture. The principle of the construction is that the IC chip is bonded to a ceramic base and connections are made with fine wires to metallisation patterns that are brought out to external solderable contact pads (castellations) as shown in Figure 8.



Leadless chip carrier castellations

For the most demanding applications, where cost is not a major constraint, a three-layer construction is used with a flat gold plated lid sealed using a gold-tin solder preform. This style of package is still used for many RF devices, although cheaper alternatives have been devised, as indicated in Figure 8. Glass sealing, using a pre-glassed ceramic lid with a three layer chip carrier, results in some cost saving. The use of a single layer chip carrier having a pre-glassed cavity and a ceramic cup-shaped lid gives a device of about half the price. Even further economies are obtained, if there is no need for hermeticity, by encapsulating the device on its ceramic base, in epoxy resin.

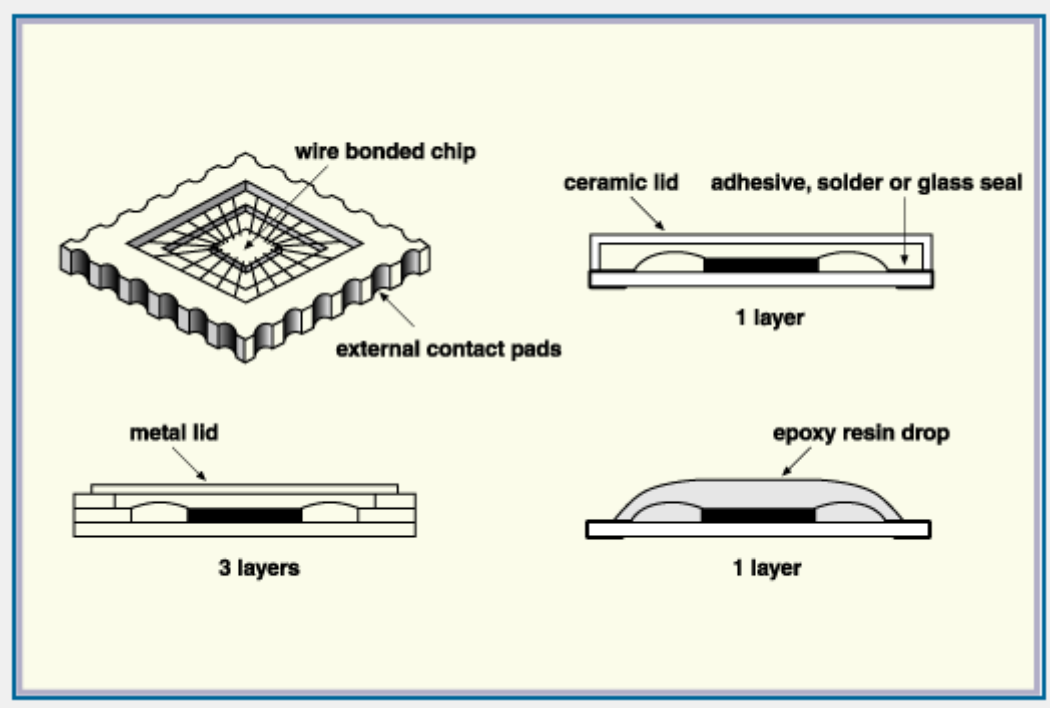
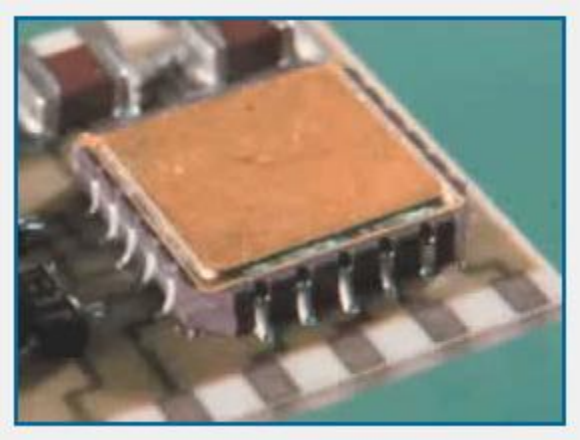


Figure 8: LCCC construction, showing three types of enclosure



Leadless chip carrier mounted on a ceramic substrate

LCCCs were originally designed to be soldered to the ceramic substrate of hybrid circuits. In this application the thermal expansion coefficients of substrate and component are matched, but this is not the case with assemblies on FR-4 laminate. Consequently, for PCB applications, the LCCC has been superseded by devices with compliant leads, to compensate for CTE mismatch between the component and the board.

The Plastic Leaded Chip Carrier

Plastic leaded chip carriers (PLCCs) are manufactured by fully automated high volume processes. The methods of die bond, wire bond and transfer moulding are conceptually exactly the same as for the SOT-23, although the number of bonds and mould complexity are both much greater, with standard packages ranging from 20 to 84 leads with dimensions up to 30 mm square. As shown in Figure 9, leads have a ‘J’ shape, folded underneath the package to save board space.

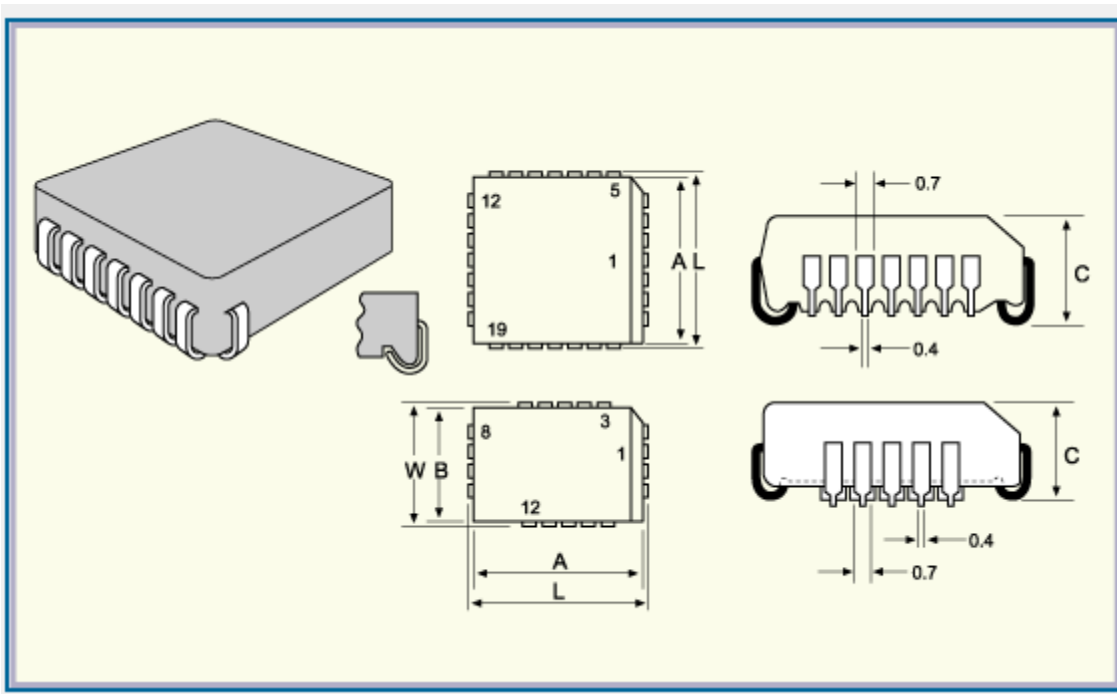
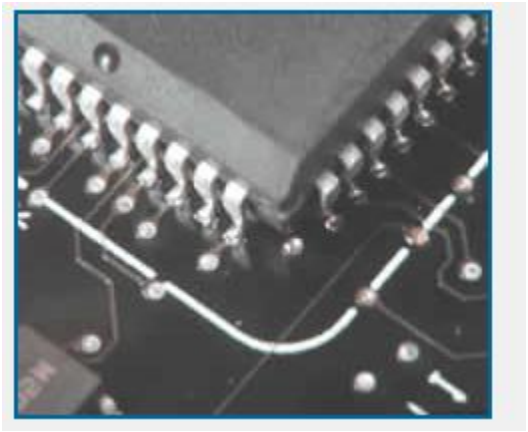


Figure 9: Lead form of a J-leaded PLCC



J-leaded PLCC

Any gain in component density may, however, be paid for by problems in wave soldering (skipped joints), in reflow soldering (wicking), and in increased difficulties at inspection (which requires oblique viewing optics) and electrical test (difficult probe access to leads). There are also mechanical limitations in forming leads on smaller pitch centres, although fine-pitch SOP equivalents with J-leads (SOJ packages) have been produced for memory devices.

The leads of most PLCCs are on a standard 1.27 mm pitch, with package sizes and formats similar to the LCCC. The leads are intended to be sufficiently compliant to accommodate any thermal expansion mismatch between the component and the PCB, and are commonly made of a copper alloy with a plated tin-lead coating to ensure good solderability.

Ball grid arrays

The increase in die complexity which has driven the electronics revolution in recent years has been mirrored by an increase in the number of lead-outs per device. For surface mount devices, this was first accommodated both by using all four sides of the packages, and by reducing the lead pitch progressively from 0.1 inch to 0.05 inch to 0.025 inch centres. This trend was fuelled by improvements in solder paste, printing and component placement, and 'fine pitch devices' were introduced, first at 0.5 mm and then at 0.4 mm pitch, with some parts even produced with leads at 0.3 mm centres.

Unfortunately, with practical circuits, there are problems in meeting the fine-pitch requirement and at the same time depositing enough solder paste for larger parts. More seriously, defect rates (typically open circuits and bridges) increase markedly at the finest pitches, and few companies routinely handle parts with pitches less than 0.4 mm.

The concept of an 'area array', where connections are not confined to the periphery of the package had already been proven with the through-hole Pin Grid Array. The rationale for the area array is that, compared to edge leads, this design allows many more connections to be made at the same pitch in the same area or, conversely, the same number of connections to be made in the same area with a greater spacing between connections. Having a coarser pitch improves yield and widens the process window.

The Ball Grid Array (BGA) adapts the earlier through-hole package by having solder balls or columns instead of pins, and reflowing them onto the board, rather than inserting and wave-soldering. BGA is, however, a generic concept, not a specific product – the only common features are that all BGAs have:

some means of chip attach and interconnect to

a mini-substrate chip carrier, sometimes referred to as an 'interposer', with

balls or columns of solder or polymer underneath, and

some means of chip protection or encapsulation

The most common construction is the type of Polymer Ball Grid Array (PBGA) represented by the Motorola OMPAC (Figure 10). This uses epoxy die attach and gold wire bonding, with an interposer of 'BT resin' laminate for higher Tg, transfer moulded single-sided encapsulation, and eutectic solder balls on 1.27 mm pitch.

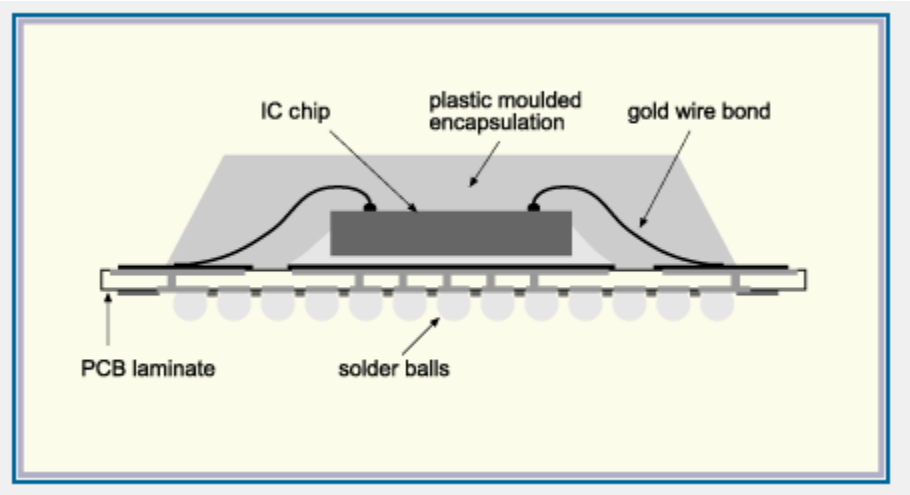
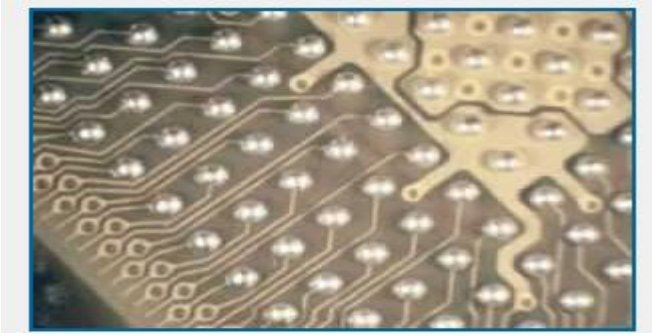


Figure 10: Example of a Polymer Ball Grid Array

A BGA built on a thin PCB



Ball terminations on a PBGA device

The term PBGA encompasses a variety of techniques, for example with TAB or flip-chip replacing wire bonding, and a 'glob-top' polymer encapsulation instead of transfer moulding, but there are many other package formats. One which is significantly different in terms of cost and reliability is the IBM standard 'column' BGA. This is designed to minimise internal TCE differences, and also reduce the stresses both by under-filling with adhesive and by increasing the stand-off between interposer and board. The CBGA uses flip-chip die attach onto an alumina or low-temperature co-fired ceramic interposer, and columns of 90:10 Pb:Sn high-melting solder on the package which are not completely dissolved in the eutectic solder on the substrate.

Ceramic Ball Grid Array termination

Thinner, smaller packages

The rapid growth in surface mount has spawned a number of packages which are relatively thinner and smaller than their standard counterparts. These packages have been developed to meet two types of requirement:

For applications such as memory products, where the die is large but the number of leads needed is comparatively small. Examples are the TSSOP (thin, shrink SO package) and the SOJ (J-leaded SO package)

For high pin count circuits, where area arrays of lead-outs are more effective than peripheral arrangements. The Ball Grid Array (BGA) is a common example of such a package. Many modern package variants are substantially thinner than the OMPAC.

The ‘Tape BGA’ a thinner form of the BGA package

This topic is one of the subjects of the Technology Awareness module. At this stage, the key point to make about such packages is that they are usually more fragile than their conventional package equivalents, and need more attention to handling and process control.

Chip-Scale Packages

Over the past 10 years a number of different packaging approaches have been used to create smaller building blocks for surface mount assembly. The aim is to have a package which does not add significantly to the area occupied by die: IPC define a ‘Chip Scale Package’ (CSP) as one where the area is less than 1.5 times that of the die (linear dimensions less than 1.2 times). Some CSPs are based on direct chip mounting, some on flip chip, and others on TAB: overall, the package may take a wide variety of different forms, but the improvement in size which can be achieved is shown dramatically in Figure 11.

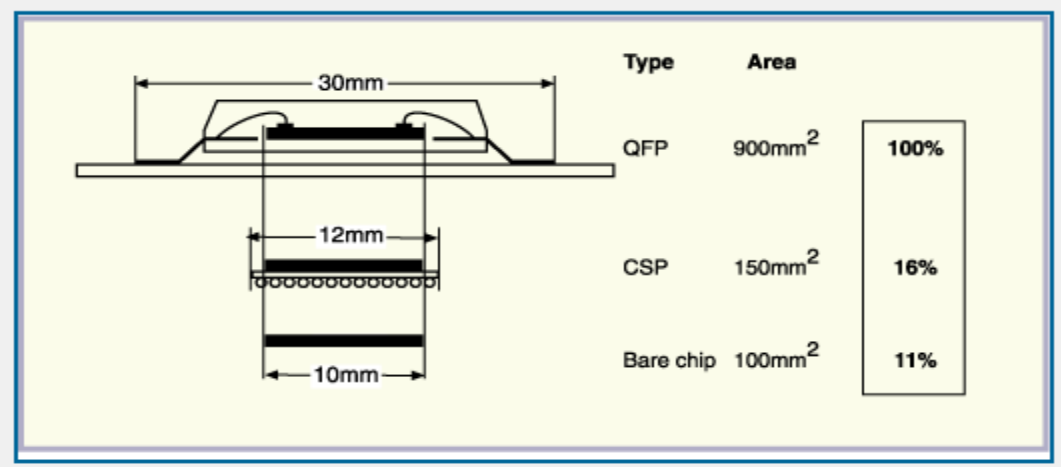


Figure 11: The advantage of Chip Scale

Author: Martin Tarr

Source: http://www.ami.ac.uk/courses/topics/0134_sp/index.html