International Journal of Electronic Engineering Research
ISSN 0975 - 6450 Volume 1 Number 3 (2009) pp. 213–221

http://www.ripublication.com/ijeer.htm

Efficiency Analysis of Bridgeless PFC Boost Converter with the Conventional Method

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Abstract

Conventional boost PFC suffers from the high conduction loss in the input rectifier-bridge. Higher efficiency can be achieved by using the bridgeless boost topology. The efficiency of various PFC topologies is studied based on its classification. Two types of PFC topology classification are proposed namely the full-bridge with 1 DC/DC converter and a Bridgeless converter. PFC circuit with low power application is the main concern in this study. In this paper, a detailed description of the operation of the proposed circuit is given. Based on the analysis, the component selection is presented. The most commonly methods used to calculate the power losses is discussed and compared for the various topologies.

Keywords: PFC, efficiency, converter.

Introduction

The efficiency of various circuit topologies has gained interest among switch-mode power supplies (SMPS) designer. High efficiency has always been one of the main concerns in developing new SMPS circuits. Besides having the capability to operate at universal input voltage, the SMPS must also comply with several standards required by industries, namely IEC 61000-3-2 which is a European standard for harmonics content. In addition, other standards such as Environmental Protection Agency (EPA), Green Grid and Climate Savers are mainly concern on energy efficiency [1]. To comply with such standards, an active power factor correction (PFC) circuit is used to eliminate the low order harmonics content and also improve the power factor and at the same time regulate the output voltage. On the other hand, the insertion of PFC circuit will in turn increase the number of components used and affects the efficiency of the SMPS in a small amount. Basically, the PFC circuits consist of semiconductor devices (MOSFET and diode), inductor and capacitor. The

component counts would depend on the PFC topology being used. Recently, standards on energy efficiency have been revised and more stringent requirements have been proposed [2]. One of the requirements is to increase the requirement for SMPS such that all SMPS should have efficiency greater than 80% during operation between 20% and 50% of its full loads.

Normally, most SMPS are rated based on full load operation. This range of load is chosen due to the fact that it is the nominal operation of most SMPS for servers and computers. Thus, the purpose of this work is to study the efficiency of several latest single-phase PFC topologies based on two categories which are: - (1) Full-bridge with 1 DC/DC converter, and (2) Bridgeless converter. Several issues will be highlighted and most of them are concerned on the efficiency of the converter at low power operation which is 300W or less.

Circuit Topology

The efficiency of several PFC circuit based on its topology will be the main issue in this paper. As mentioned earlier, the efficiency of the converter will be studied based on which topologies it falls. The work will only consider the single-stage PFC converters. The justification for this statement is defined in [3], whereby a single-stage converter is a class of converter which requires only one control signal that can be used to control a switch or a set of switches in that particular circuit or systems. Thus, it means that the number of stage(s) doesn't directly determine by the number of converter that the circuit has. In general, there are two types of power loss measurement exist namely the electrical measurement and calorimetric measurement [4, 5]. Normally, the electrical measurement is used to calculate the power losses by measuring the value of voltage and current flowing across and through the device. On the other hand, it is also possible to calculate the power losses by measuring the difference of the power at the input to the output. This method is the most popular and easiest way to determine the power losses and efficiency across a device or a system. However, the drawback of this technique is the power losses value is not as accurate as the calorimetric measurement but it is still within the acceptable practical value.

The electrical measurement is found to be the easiest and most used technique to measure the losses of a device or a circuit. The calorimetric is found to be one of the most accurate power loss measurements. Basically, this technique will measure the losses of any individual device. Unfortunately, it is found that this method is not suitable in measuring losses of power electronics circuit due to several factors such as the arrangement of the devices in PCB in such a way will affect the losses of any device near to it. On top of that, this method takes long time to be executed and really difficult on the arrangement using measurement [5]. Recently, a novel method in measuring power losses using temperature measurement has been proposed in [5]. In this measurement, the losses of each device are calculated by matching the temperature of the converter running at operating point and testing the individual devices. It is reported that this measurement technique is more accurate compared to the electrical measurement.

A. Full-bridge with 1 DC/DC converter

In this topology, only one DC/DC converter is used, and that's the reason why this topology is classified as single-stage PFC. Figure 01: shows the general circuit diagram for single-stage PFC circuit. The DC/DC converter is always known as Power Factor Pre-regulator (PFC). It can be seen that the PFP is the only controllable device in this circuit and thus PFP is used to reshape the input current and to regulate the output voltage as well. Several DC/DC converters have been used as PFP and the performance of the PFC circuit is solely depending on the capability of the PFP. The most popular PFC which is known as Single-stage Boost PFC falls in this category. Figure 2.2(b) shows the circuit diagram of Boost PFC circuit which has lately gained some interest especially in improving its performance [8]-[1]. The work in [8] concentrates on the effect of introducing snubber circuit to the efficiency of the converter operated in DCM. The losses due to the RC snubber circuit can be calculated as,

$$P_s = f_{SW} C_{SN} Vo^2 \qquad \text{------- (1)}$$

where f_{SW} is the switching frequency,
C_{SN} is the snubber capacitor and
v_O is the output voltage.

The snubber circuit is connected in parallel with the MOSFET. However, it is found in this work that by using a properly designed RCD snubber, the switching losses is halves compared to the losses when RC snubber operated at critically damped response is used. The best efficiency is obtained when no snubber circuit is used. It can be concluded that the insertion of the snubber circuit doesn't seem to give a good impact on the efficiency of the circuit although the switching losses. As reported in [1], the performance of silicon carbide (SiC) diode used in Boost PFC is observed. Comparison between SiC diode and two ultra-fast plus soft-recovery silicon diodes are made.

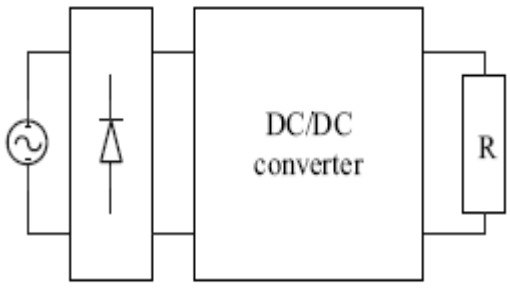

Figure 01: Converter arrangement for full-bridge rectifier with 1DC/DC converter

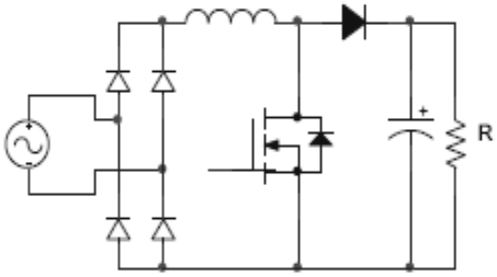

Figure 02: Boost PFC

The conventional converter model is simulated and shown in Fig 03. The corresponding input wave form is shown in fig 04 and output voltage waveform is shown in fig 05.In this work, universal input voltage and 300W output voltage are the specifications determined to test the three devices performances. It is reported that the efficiency of Boost PFC with SiC diode is 97% and 93% for 220Vrms and 110Vrms input respectively. The efficiencies of the other two diode is reported lower at 96.4% and 95.5% at 220Vrms while at 110Vrms input voltage, the efficiencies are 92% and 91%.

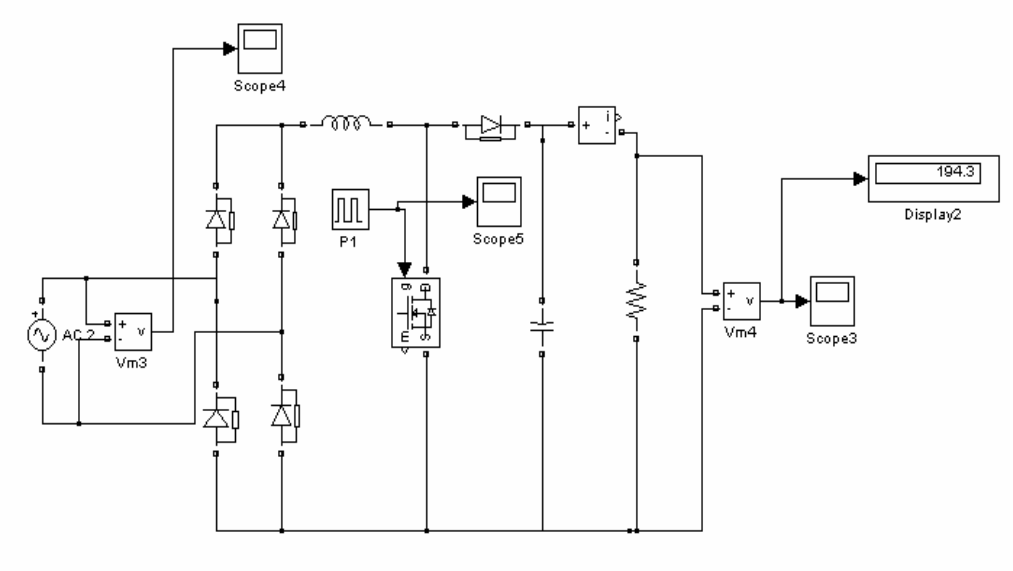

Figure 03: Simulink model of Conventional Converter.

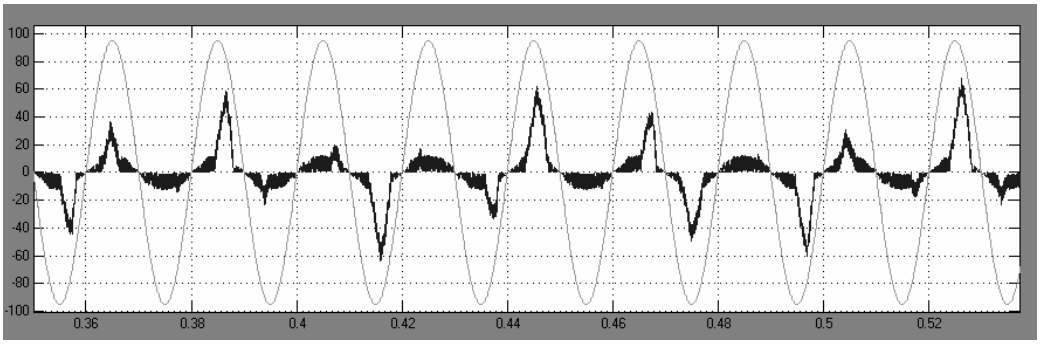

Figure 04: Input waveform.

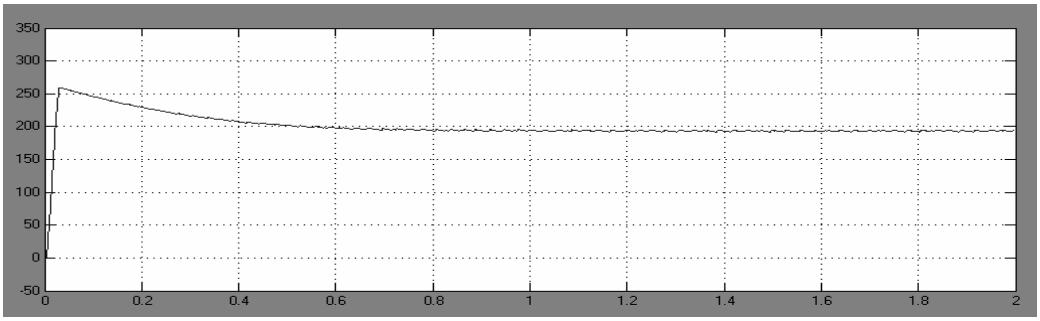

Figure 05: DC output waveform.

A newly proposed PFC circuit is presented in [1] consist of a Flyback converter with synchronous rectifier circuit. Actually, this circuit is based on modified Boost PFC with high-frequency transformer which is used to step down the voltage to 19V DC. The circuit is tested in DCM mode with output power ranging from 10W to 90W and also with universal input mains which in turns reflect the application of computer adapters. The switching frequency is varies between 30-70 kHz, in which lower switching frequency is for lower input voltage and vice versa for higher switching frequency. It seems that during operation at 10W output power, this topology shows 87% and 85% efficiency for 120Vrms and 230Vrms input voltage respectively and increase to 90% at 20W for both voltage. The efficiency will increase further at higher loads. At full load which is at 90W, the efficiency is 93% and 94% for 120Vrms and 230Vrms input voltage respectively.

B. Bridgeless converter

As shown in Fig 06, the Bridgeless topology does not have rectifier circuit operated throughout the full cycle and that's the reason for its name. Figure 2.3(b) shows one of the earliest topology in this class which is called the Bridgeless Boost PFC; proposed in [2]. The Bridgeless PFC converter has recently gaining its popularity in giving high efficiency and high performance converter. The work reported in [3] shows several Bridgeless PFC topologies and it is found that only two topologies are suitable for practical purposes. One of these topologies has been tested in continuous-conduction mode (CCM) and DCM/CCM boundary conditions with universal input voltage and has been discussed extensively in terms of practical views.

The corresponding output voltage is shown in the Fig 10. The switching frequency for CCM is 110 kHz and for CCM/DCM boundary region is varies between 85-400 kHz. The losses of main component is tabulated and compared with the conventional Boost PFC circuit. It can be concluded that at 300W in DCM/CCM boundary, the efficiency between conventional PFC and Bridgeless PFC differ by less than 1%; i.e. 96.2% for conventional PFC and 97% for Bridgeless PFC. At lower power operation which is all the way down from 300W to 50W, the efficiency gap between those two PFC converter is widen. As can be observed at 150W, the efficiency gap is almost

1.25%, i.e. 96% efficiency for conventional PFC and 97.2% for Bridgeless PFC. At 50W loads, the efficiency for conventional PFC is recorded at 90.5% and 95.2% efficiency is recorder for Bridgeless PFC resulting 5.2% gap on the efficiency. On top of that, the efficiency of DCM/CCM boundary is better compared to the CCM operation at same power level.

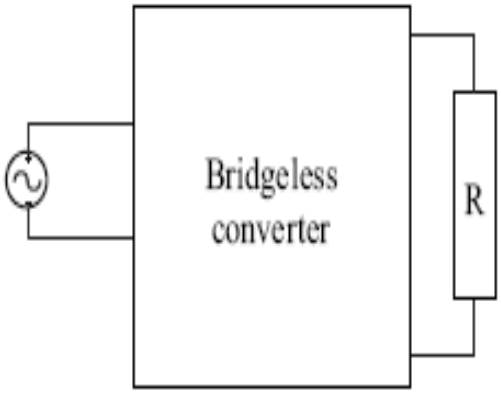

Figure 06: Converter arrangement for Bridgeless converter.

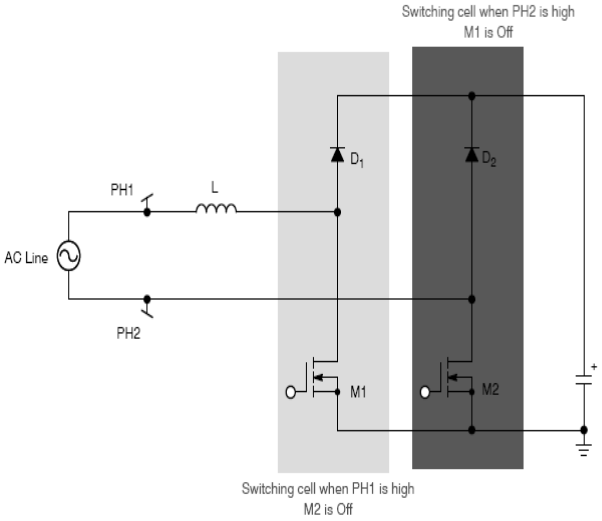

Figure 07: Bridgeless Boost PFC.

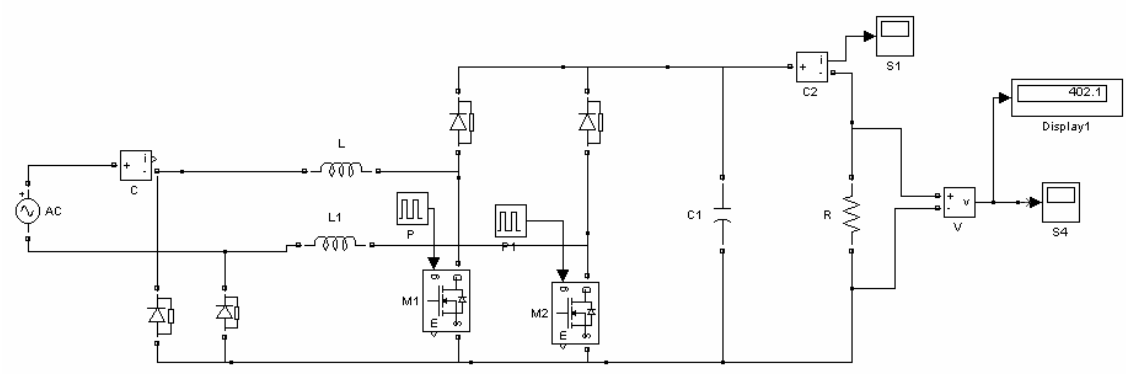

Figure 08: Simulink model of Bridgeless Boost PFC.

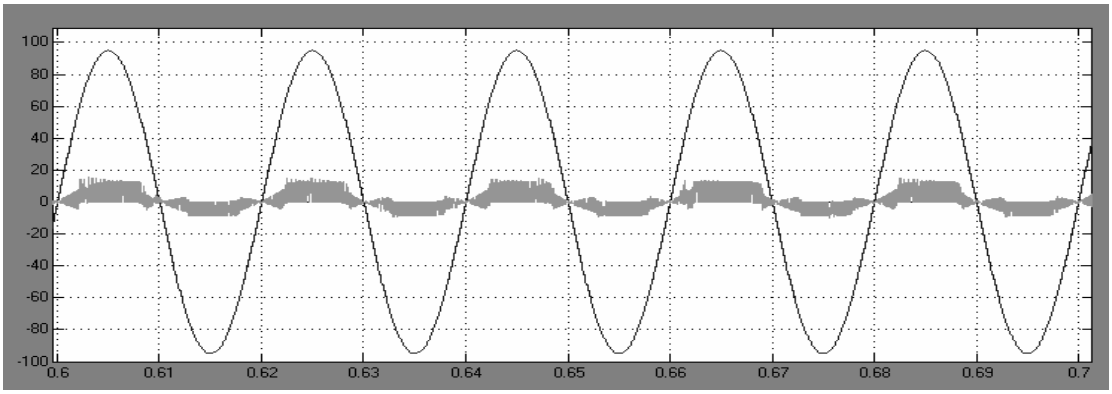

Figure 09: Ac input voltage and current.

The Simulink model of Bridgeless PFC is shown in Fig 08.The AC input voltage and current wave forms of Bridgeless Circuit is shown in Fig 09:

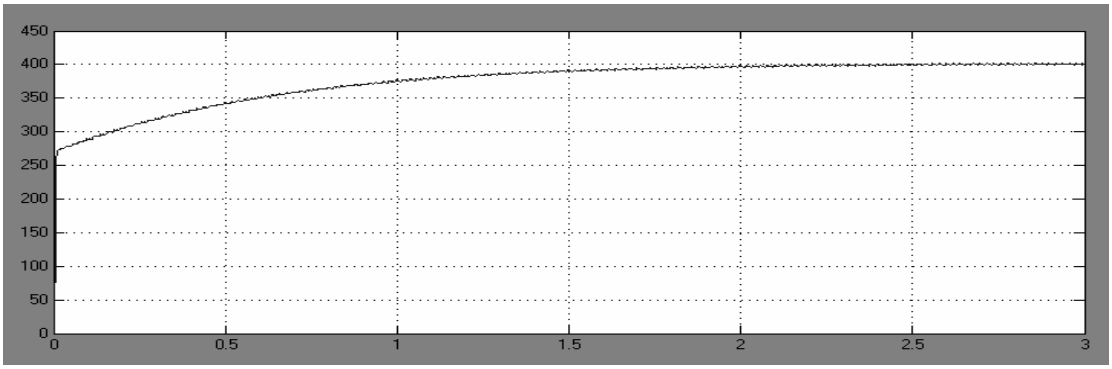

Figure 10: Output voltage waveform

Besides the works discussed so far, there are still many circuits that have been tested showing the high efficiency characteristic inherent the Bridgeless PFC circuit [5]- [8]. As can be seen in Fig 11, a comparison is made using the data obtained in each paper and the efficiency during low power operation is concerned. As discussed earlier, future SMPS require the efficiency of the converter should exceed 80% during low load operation which is 20% to 50% of full loads. The converters discussed in [7], [8] and [1] are suitable for SMPS due to its output voltage regulated at 56V, 48V and 19V respectively. In the Fig 11, a slightly better efficiency is achieved in [1] which fall in second category, ‘full-bridge with 1 DC/DC converter’.

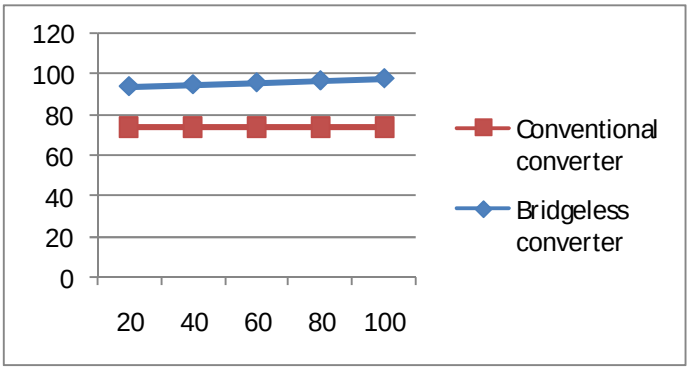

Figure 11: Comparison of Bridgeless and Conventional topology on their efficiency.

This converter is ready to be used as SMPS due to its output voltage already regulated at 19V. Efficiency of this converter is tabulated above 90% for all loads condition. The efficiency of Bridgeless circuit discuss in [3] surpassing the other topologies with projected efficiency ranging between 94% and 96% throughout all loads. However, this converter cannot be compared directly with three circuits discussed earlier due to its output voltage value which is not catered for SMPS applications. In [3], the output voltage is regulated at 390V and 400V but an SMPS requires the output voltage to be around 19V.

Conclusions

Based on the Two PFC topologies, it is found that the best efficiency is obtained from the Bridgeless topology followed by the full-bridge with 1 DC/DC converter. It is found that by using less number of components, the efficiency can be improved up to 8% and in some cases up to 10% as explained previously. However, the Bridgeless converters discussed in this paper were unable to be used as SMPS due to its output voltage which is not regulated at 19V. Thus, some work should be done to show that the Bridgeless converter can give the same results on its efficiency if it is designed to suit the SMPS requirements. Although it shows very good efficiency when the output voltage regulated at voltage around 390V but it is still a doubt that this Bridgeless converter can still giving high efficiency in SMPS environment. On the other hand, the effect of switching frequency to the converter is not being discussed extensively in most work although it is a well known fact that by increasing the switching frequency, the switching losses will increase as well. On top of that, it can be observed that several works have been using variable switching frequency especially for fully DCM or CCM/DCM boundary operation.

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