DIODE CLAMPING CIRCUITS

In this article, the working of a clamping circuit is explained. The working of different clamping circuits like positive and negative clamper, with circuit diagrams and waveforms are given below.

TRANSISTOR CLIPPING CIRCUITS

A clamping circuit is used to place either the positive or negative peak of a signal at a desired level. The dc component is simply added or subtracted to/from the input signal. The clamper is also referred to as an IC restorer and ac signal level shifter.

In some cases, like a TV receiver, when the signal passes through the capacitive coupling network, it loses its dc component. This is when the clamper circuit is used so as to re-establish the the dc component into the signal input. Though the dc component that is lost in transmission is not the same as that introduced through a clamping circuit, the necessity to establish the extremity of the positive or negative signal excursion at some reference level is important.

A clamp circuit adds the positive or negative dc component to the input signal so as to push it either on the positive side, as illustrated in figure (a) or on the negative side, as illustrated in figure (b).

The circuit will be called a positive clamper , when the signal is pushed upward by the circuit. When the signal moves upward, as shown in figure (a), the negative peak of the signal coincides with the zero level.

The circuit will be called a negative clamper, when the signal is pushed downward by the circuit. When the signal is pushed on the negative side, as shown in figure (b), the positive peak of the input signal coincides with the zero level.

POSITIVE CLAMPING AND NEGATIVE CLAMPING

(a) Positive clamping

(b) Negative clamping

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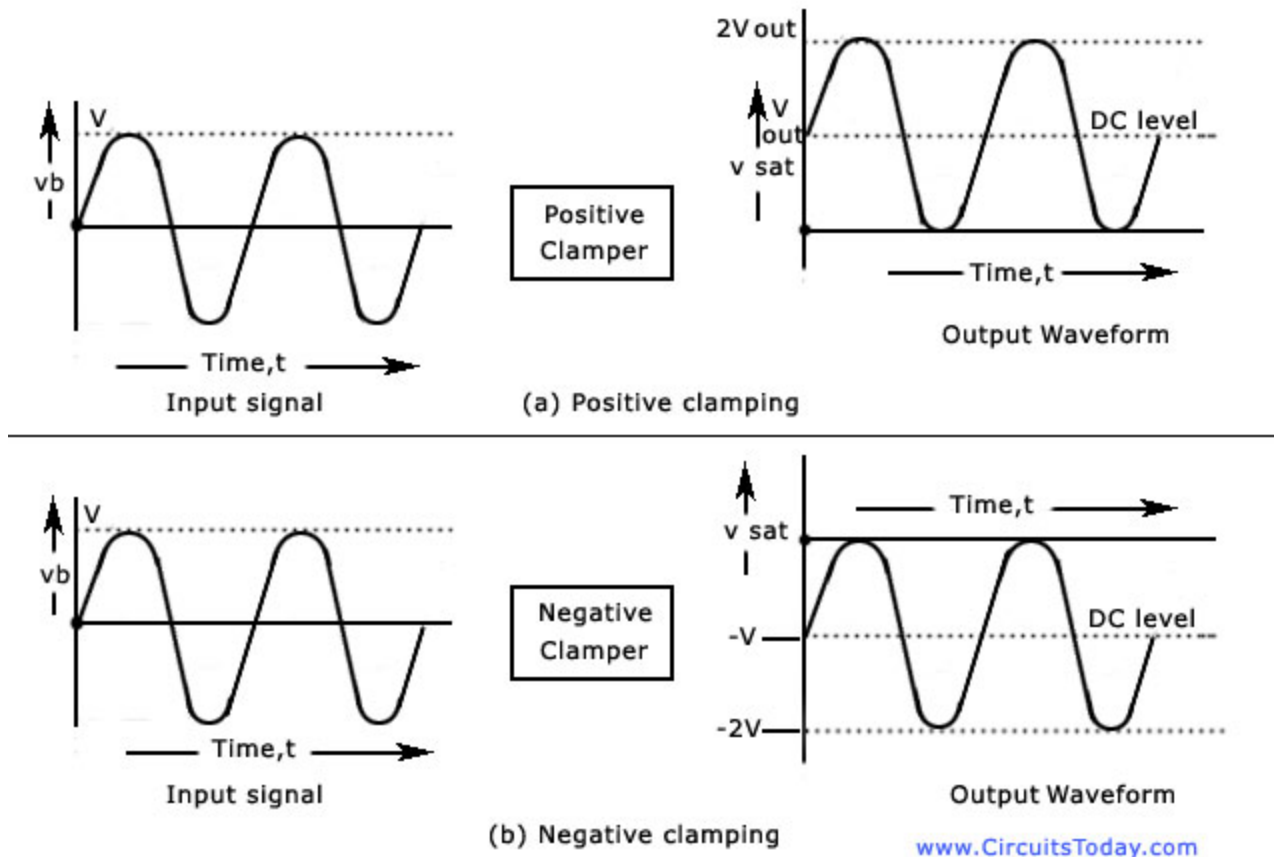
For a clamping circuit at least three components — a diode, a capacitor and a resistor are required. Sometimes an independent dc supply is also required to cause an additional shift. The important points regarding clamping circuits are:

(i) The shape of the waveform will be the same, but its level is shifted either upward or downward,

(ii) There will be no change in the peak-to-peak or rms value of the waveform due to the clamping circuit. Thus, the input waveform and output waveform will have the same peak-to-peak value that is, $2V_{max}$. This is shown in the figure above. It must also be noted that same readings will be obtained in the ac voltmeter for the input voltage and the clamped output voltage.

(iii) There will be a change in the peak and average values of the waveform. In the figure shown above, the input waveform has a peak value of V_{max} and average value over a complete cycle is

zero. The clamped output varies from 2 V_{max} and 0 (or 0 and -2V_{max}). Thus ths peak value of the clamped output is 2V_{max} and average value is $V_{max.}$

(iv) The values of the resistor R and capacitor C affect the waveform.

(v) The values for the resistor R and capacitor C should be determined from the time constant equation of the circuit, t = RC. The values must be large enough to make sure that the voltage across the capacitor C does not change significantly during the time interval the diode is non-conducting. In a good clamper circuit, the circuit time constant t = RC should be at least ten times the time period of the input signal voltage.

It is advantageous to first consider the condition under which the diode becomes forward biased.

Clamping circuits are often used in television receivers as dc restorers. The signal that is sent to the TV receiver may lose the dc components after being passed through capacitively coupled amplifiers. Thus the signal loses its black and white reference levels and the blanking level. Before passing these signals to the picture tube, these reference levels have to be restored. This is done by using clamper circuits. They also find applications in storage counters, analog frequency meter, capacitance meter, divider and stair-case waveform generator.

Consider a negative clamping circuit, a circuit that shifts the original signal in a vertical downward direction, as shown in the figure below. The diode D will be forward biased and the capacitor C is charged with the polarity shown, when an input signal is applied. During the positive half cycle of input, the output voltage will be equal to the barrier potential of the diode, V_0 and the capacitor is charged to (V – V_Q). During the negative half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage. The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to – V – (V — V_0) or – (2 V – V_0). The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to V_0-[-(2V-V_0)]   or   2 V.

The figure shown below can me modified into a positive clamping circuit by reconnecting the diode with reversed polarity. The positive clamping circuit moves the original signal in a vertical upward direction. A positive clamping circuit is shown in the figure below. It contains a diode D and a capacitor C as are contained in a negative clamper. The only difference in the

circuit is that the polarity of the diode is reversed. The remaining explanation regarding the working of the circuit is the same as it is explained for the negative clamper.
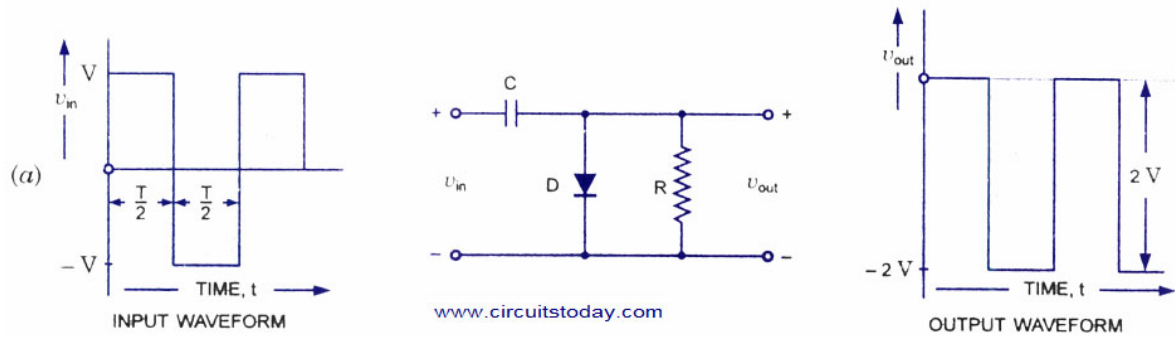
To remember which way the dc level of a signal moves, look at figure shown below. Notice that the diode arrows point downward, the same direction as the dc shift.
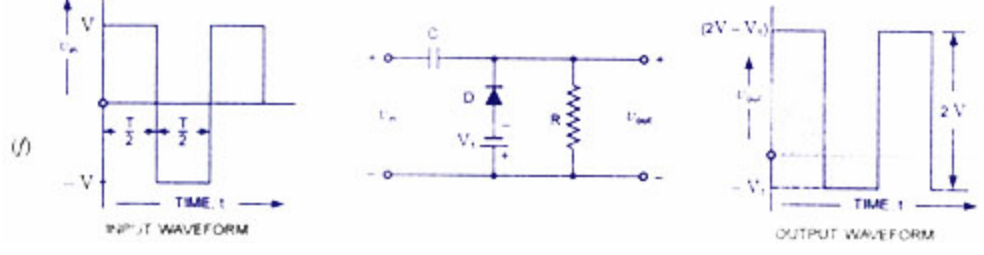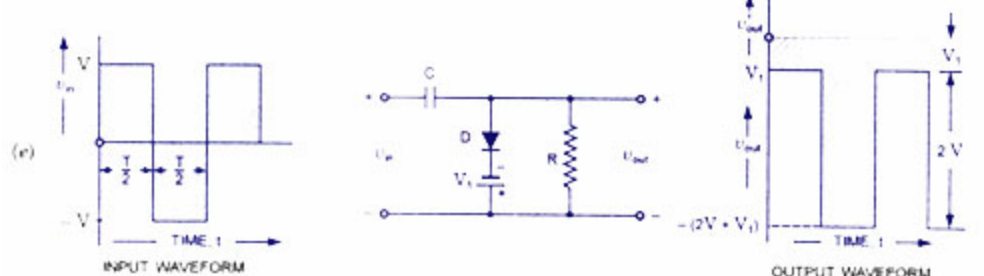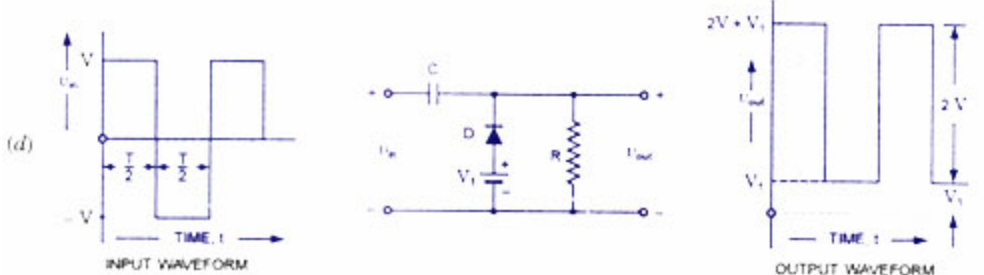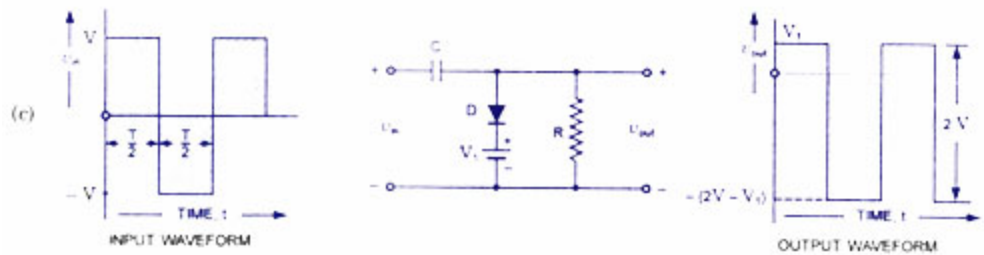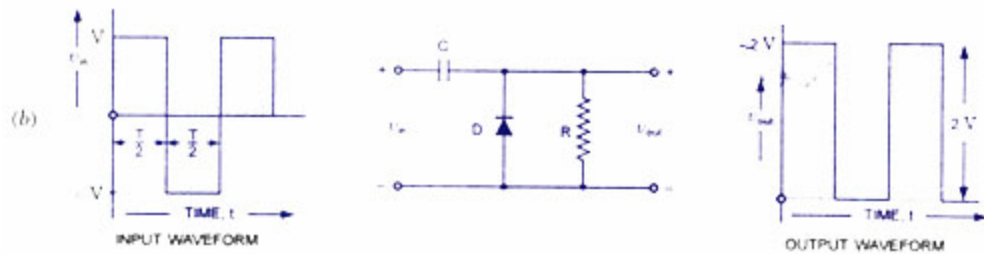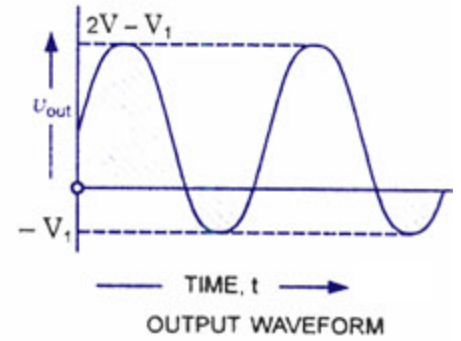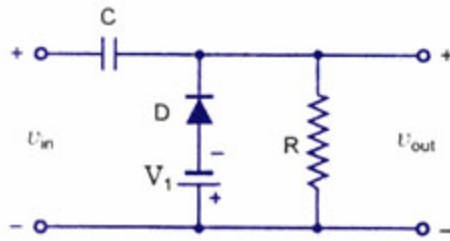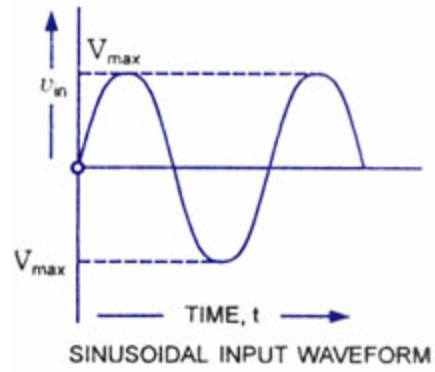

Negetive Clamping Circuit
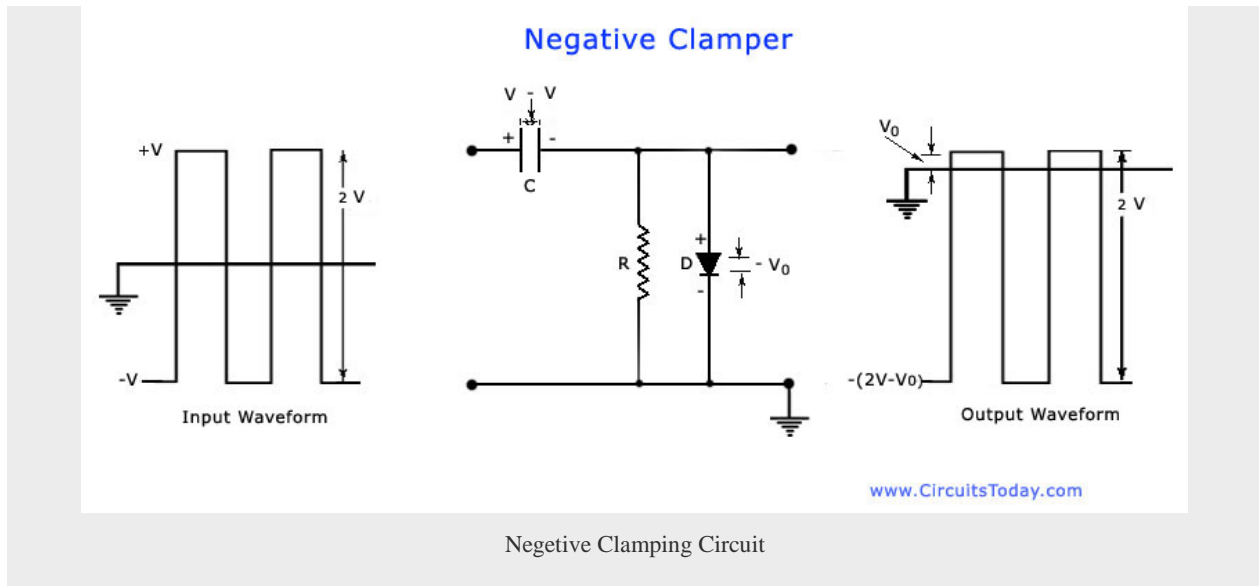
Similarly in the figure shown below, the diode arrow points upward, again the same direction as the dc shifts. It means that, when the diode points upward. We have a positive dc clamper and when the diode points downward, the circuit is a negative dc clamper.

Positive Clamping Circuit
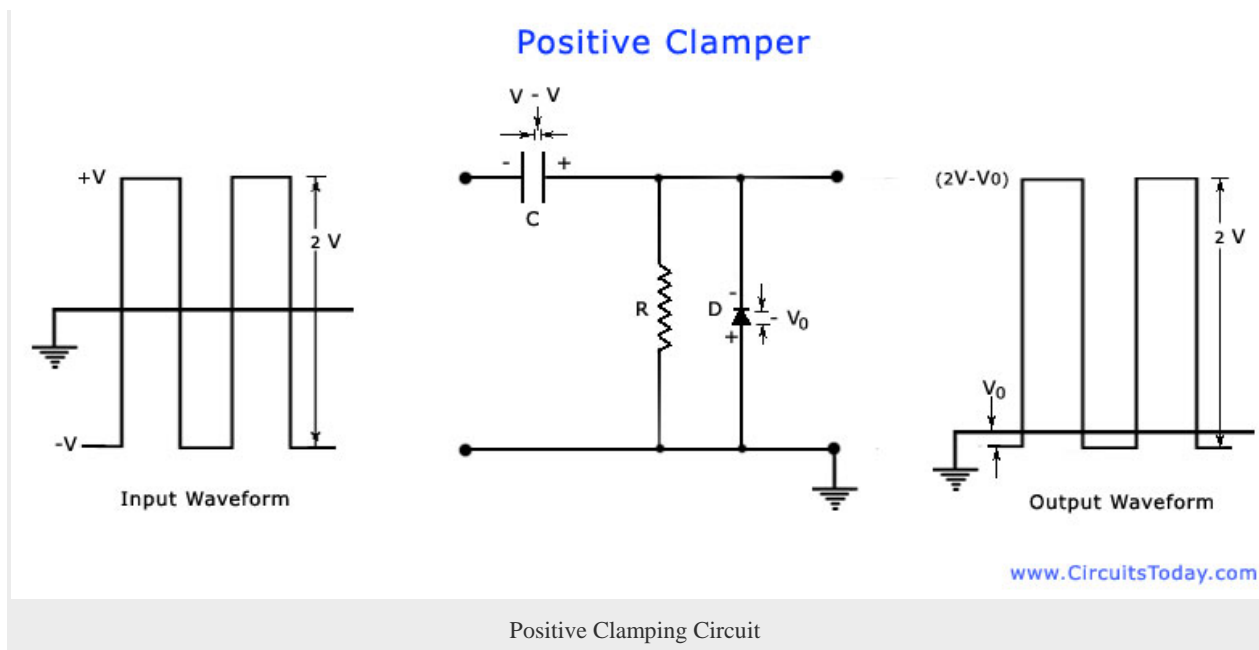
A number of clamping circuits with their effect on the input signal are shown in the figure given below. All the figures shown below have the input and output signals in square waves, the same procedure can be used for sinusoidal inputs. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal wave signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response, as illustrated in figure (g) for a network appearing in figure (f). The diodes have been assumed to be ideal and 5 RC » T/2 in drawing the output waveforms.

(a)

INPUT WAVEFORM

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OUTPUT WAVEFORM

(b)

v_{in}
V
$\frac{T}{2}$ $\frac{T}{2}$
$-V$
TIME, t
INPUT WAVEFORM

C
D R v_{out}
v_{in}

$-2\,V$
v_{out}
2 V
TIME, t
OUTPUT WAVEFORM

(c)

v_{in}
V
$\frac{T}{2}$ $\frac{T}{2}$
$-V$
TIME, t
INPUT WAVEFORM

C
D R v_{out}
V_1
v_{in}

V_1
v_{out}
2 V
$-(2V - V_1)$
TIME, t
OUTPUT WAVEFORM

(d)

v_{in}
V
$\frac{T}{2}$ $\frac{T}{2}$
$-V$
TIME, t
INPUT WAVEFORM

C
D R v_{out}
V_1
v_{in}

$2V + V_1$
v_{out}
2 V
V_1
V_1
TIME, t
OUTPUT WAVEFORM

(e)

v_{in}
V
$\frac{T}{2}$ $\frac{T}{2}$
$-V$
TIME, t
INPUT WAVEFORM

C
D R v_{out}
V_1
v_{in}

v_{out}
V_1
V_1
v_{out}
2 V
$-(2V + V_1)$
TIME, t
OUTPUT WAVEFORM

(f)

v_{in}
V
$\frac{T}{2}$ $\frac{T}{2}$
$-V$
TIME, t
INPUT WAVEFORM

C
D R v_{out}
V_1
v_{in}

$(2V - V_1)$
v_{out}
2 V
$-V_1$
TIME, t
OUTPUT WAVEFORM

Different Clamping Circuits

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