

# DIFFERENCE BETWEEN A LATCH AND A FLIP-FLOP

- Both latches and flip-flops are circuit elements whose output depends not only on the present inputs, but also on previous inputs and outputs.
- They both are hence referred as "sequential" elements.
- In electronics, a latch, is a kind of bistable multi vibrator, an electronic circuit which has two stable states and thereby can store one bit of information. Today the word is mainly used for simple transparent storage elements, while slightly more advanced non-transparent (or clocked) devices are described as flip-flops. Informally, as this distinction is quite new, the two words are sometimes used interchangeably. [wiki]
- In digital circuits, a flip-flop is a kind of bistable multi vibrator, an electronic circuit which has two stable states and thereby is capable of serving as one bit of memory. Today, the term flip-flop has come to generally denote non-transparent (clocked or edge-triggered) devices, while the simpler transparent ones are often referred to as latches.[wiki]
- A flip-flop is controlled by (usually) one or two control signals and/or a gate or clock signal.
- Latches are level sensitive i.e. the output captures the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes.
- Flip-Flops are edge sensitive i.e. flip flop will store the input only when there is a rising or falling edge of the clock.
- A positive level latch is transparent to the positive level(enable), and it latches the final input before it is changing its level(i.e. before enable goes to '0' or before the clock goes to -ve level.)
- A positive edge flop will have its output effective when the clock input changes from '0' to '1' state ('1' to '0' for negative edge flop) only.
  
- Latches are faster, flip flops are slower.
- Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches.
- Latches take less gates (less power) to implement than flip-flops.
- D-FF is built from two latches. They are in master slave configuration.
- Latch may be clocked or clock less. But flip flop is always clocked.
- For a transparent latch generally D to Q propagation delay is considered while for a flop clock to Q and setup and hold time are very important.

## Synthesis perspective: Pros and Cons of Latches and Flip Flops

- In synthesis of HDL codes inappropriate coding can infer latches instead of flip flops. Eg.: "if" and "case" statements. This should be avoided sa latches are more prone to glitches.

- Latch takes less area, Flip-flop takes more area ( as flip flop is made up of latches) .
- Latch facilitate time borrowing or cycle stealing whereas flip flops allow synchronous logic.
- Latches are not friendly with DFT tools. Minimize inferring of latches if your design has to be made testable. Since enable signal to latch is not a regular clock that is fed to the rest of the logic. To ensure testability, you need to use OR gate using "enable" and "scan\_enable" signals as input and feed the output to the enable port of the latch. [ref]
- Most EDA software tools have difficulty with latches. Static timing analyzers typically make assumptions about latch transparency. If one assumes the latch is transparent (i.e.triggered by the active time of clock,not triggered by just clock edge), then the tool may find a false timing path through the input data pin. If one assumes the latch is not transparent, then the tool may miss a critical path.
- If target technology supports a latch cell then race condition problems are minimized. If target technology does not support a latch then synthesis tool will infer it by basic gates which is prone to race condition. Then you need to add redundant logic to overcome this problem. But while optimization redundant logic can be removed by the synthesis tool ! This will create endless problems for the design team.
- Due to the transparency issue, latches are difficult to test. For scan testing, they are often replaced by a latch-flip-flop compatible with the scan-test shift-register. Under these conditions, a flip-flop would actually be less expensive than a latch. Read a good article on problems of latch published in eetimes long back !!
- Flip flops are friendly with DFT tools. Scan insertion for synchronous logic is hassle free.

Source : <http://asic-soc.blogspot.in/2008/01/what-is-difference-between-latch-and.html>