DELAYS IN ASIC DESIGN

We encounter several types of delays in ASIC design. They are as follows:

- Gate delay or Intrinsic delay
- Net delay or Interconnect delay or Wire delay or Extrinsic delay or Flight time
- Transition or Slew
- Propagation delay
- Contamination delay

Wire delays or extrinsic delays are calculated using output drive strength, input capacitance and wire load models. Other delays are intrinsic properties of each and every gate.

Delays are interdependent on different electrical properties. [Nekoogar]:

- Input capacitance of the logic gate is a function of output state, output loads and input slew rate.
- Internal timing arcs and output slew rate is a function of switching input(s).
- Capacitance of the wire is dependent on frequency.

- Internal timing arcs are a function of input slew rates.
- Output slew rate is a function of input slew rate on each input.
- Wires exhibit RLC characteristics instead of lumped RC.

Gate Delay

Transistors within a gate take a finite time to switch. This means that a change on the input of a gate takes a finite time to cause a change on the output. [Magma]

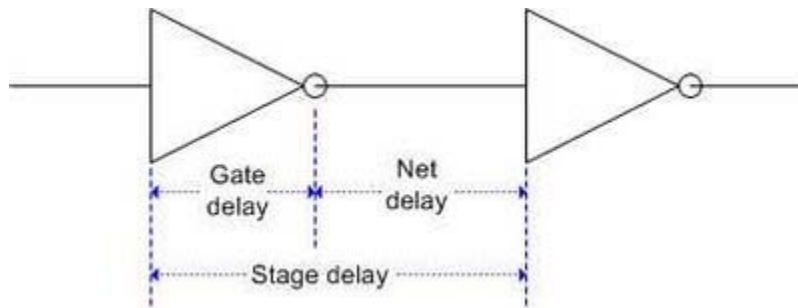**Gate delay =function of (input transition (slew) time, Cnet+Cpin).**

or

Gate delay =function of (input transition (slew) time, Cload).

where Cload=Cnet+Cpin

Cnet-->Net capacitance

Cpin-->pin capacitance of the driven cell

Cell delay is also same as Gate delay.

How gate delay is calculated?

Cell or gate delay is calculated using **Non-Linear Delay Models (NLDM)**. NLDM is highly accurate as it is derived from SPICE characterizations. T**he delay is a function of the input transition time (i.e. slew) of the cell, the wire capacitance and the pin capacitance of the driven cells.** A slow input transition time will slow the rate at which the cell's transistors can change state logic 1 to logic 0 (or logic 0 to logic 1), as well as a large output load **Cload (Cnet + Cpin)**, thereby increasing the delay of the logic gate.

There is another NLDM table in the library to calculate output transition. Output transition of a cell becomes the input transition of the next cell down the chain.

- Table models are usually two-dimensional to allow lookups based on the **input slew** and the **output load (Cload)**. A sample table is given below.

timing() {

related_pin : "CKN";

timing_type : falling_edge;

timing_sense : non_unate;

```
cell_rise(delay_template_7x7) {

index_1 ("0.012, 0.032, 0.074, 0.154, 0.318, 0.644, 1.3");

index_2 ("0.001278, 0.0046008, 0.0112464, 0.0245376, 0.05112, 0.10454, 0.212148");

values ( \

"0.225894, 0.249015, 0.285537, 0.352680, 0.484244, 0.748180, 1.279570", \

"0.231295, 0.254415, 0.290938, 0.358081, 0.489646, 0.753585, 1.284980", \

"0.243754, 0.266878, 0.303398, 0.370542, 0.502105, 0.766044, 1.297440", \

"0.267240, 0.290389, 0.326908, 0.394052, 0.525615, 0.789561, 1.320950", \

"0.307080, 0.330200, 0.366721, 0.433861, 0.565425, 0.829373, 1.360760", \

"0.380552, 0.403875, 0.440426, 0.507569, 0.639136, 0.903084, 1.434500", \

"0.497588, 0.521769, 0.558548, 0.625744, 0.757301, 1.021260, 1.552680");

}

rise_transition(delay_template_7x7) {

index_1 ("0.012, 0.032, 0.074, 0.154, 0.318, 0.644, 1.3");

index_2 ("0.001278, 0.0046008, 0.0112464, 0.0245376, 0.05112, 0.10454, 0.212148");

values ( \

"0.040574, 0.068619, 0.125391, 0.246672, 0.497688, 1.005982, 2.030120", \

"0.040570, 0.068618, 0.125390, 0.246672, 0.497688, 1.005940, 2.030240", \

"0.040565, 0.068616, 0.125389, 0.246650, 0.497770, 1.006180, 2.030120", \

"0.040532, 0.068612, 0.125387, 0.246670, 0.497710, 1.006164, 2.030100", \

"0.040578, 0.068621, 0.125392, 0.246636, 0.497688, 1.006182, 2.030040", \

"0.041763, 0.069211, 0.125662, 0.246758, 0.497726, 1.005930, 2.030000", \

"0.045813, 0.071321, 0.126671, 0.247154, 0.497846, 1.005962, 2.030180");

}
```

index_1 --> input transition values

index_2--> output load capacitance values

values--> delay values

Situation 1:

Input transition and output load values match with table index values

If both input transition and output load values match with table index values then corresponding delay value is directly picked up from the delay "values" table as highlighted by yellow shaded data.

Situation 2:

Output load values doesn't match with table index values

- When the actual load capacitance values does not fall directly on or at one of the load-axis index points, the delay is determined by interpolation from the closest points. Note that to carry out interpolation input transition point should match with the any one of the table index values.
- Determine the equation for the line segment connecting the two nearest points in the table.

To do this first we need to find the slope value.

Slope m = (y2-y1)/(x2-x1) where (y2-y1) is delay segment (generally in ns) on y axis and (x2-x1) is load segment (generally in pf) on x-axis.

- Solve for the delay at the load point of interest.

The linear equation is:

y = mx+c

where

y-->delay (ns)

m-->slope

x-->load capacitance (pf)

i.e. delay=slope*load point of interest (constant value is zero)

Load point of interest means load capacitance value for which delay has to be calculated.

Situation 3:

Both input transition and output load values doesn't match with table index values

- If both input transition and load capacitance values do not match exactly with the look up table index values then bilinear interpolation is used.
- Multiple linear interpolations (~3) are performed on multiple closest table data points (~4) as shown in highlighted violet color in the look up table.

Situation 4:

Output load values doesn't match with table index values and is outside the table boundary

- When the load point is outside of the boundary of the index, the delay is extrapolated to the closest known points.
- Lookup value too far out of range of the given table value could lead to inaccuracy. [Cadence]

Intrinsic delay

- Intrinsic delay is the delay internal to the gate. This is from input pin of the cell to output pin of the cell.
- It is defined as the delay between an input and output pair of a cell, when a near zero slew is applied to the input pin and the output does not see any load condition. It is caused by the internal capacitance associated with its transistor.
- This delay is largely dependent on the size of the transistors forming the gate because increasing size of transistors increase internal capacitors.