DESIGN OF A NEW DOUBLE PULSE LATCH FLIP FLOP

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***Abstract*- This paper presents a new double pulse flip flop, which is composed of a pulse generator and latch part. DPLFF consumes less power and few transistor compare to other flip-flop. As feature size of the CMOS technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip. Double pulsed latch flip flop faster than other flip flop. This design features consumes less power. In this flip flop we modified the pulse generator to suit the circuit. The double pulse latch flip-flop has symmetric timing property. TSPICE simulation result at a frequency of 400MHz shows that proposed DPLFF consume less power compare to DPSCRFF.**

***Keywords*— Flip-flop, clock skew and pulse generator.**

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I. INTRODUCTION

Flip flop is a basic memory element. Flip flop is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. A circuit incorporating flip-flops has the attribute of state its output depends not only on its current input, but also on its previous inputs. Such a circuit is described as sequential logic. Where a single input is provided, the circuit changes state every time a pulse appears on the input signal. Since the flip-flop retains the state after the signal pulses are removed, one type of flip-flop circuit is also called a "latch". Other types of flip-flops may have inputs that set a particular state, set the opposite state, or change states, depending on which input is pulsed. Flip-flops are used as data storage elements, for counting of pulses, and for synchronizing randomly-timed input signals to some reference timing signal. Flip-flops are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Double pulse latch flip-flop consist of pulse generator and latch part .The pulse generator generates the short duration pulse at the active clock edge and these pulses operate the latch part. . By reducing the transparency period of a latch to a narrow window, the latch can operate as a flip flop with the additional advantage of allowing limited time borrowing across cycle boundaries to reduce sensitivity to clock skew and jitter.

This flip flop consumes less amount of power than Conventional double pulse set conditionally reset flip-flop DPSCRFF due to less transition of internal nodes. The staking of transistor in latch stage reduces sub threshold leakage current and thus the static power consumption is also less in DPLFF.

II. CONVENTIONAL DOUBLE PULSE FLIP FLOP

Double pulse set conditional reset flip- flop

The DPSCRFF is composed of two pieces the first one is a static set reset latch and second is pulse generator. The DPSCRFF is a single ended static flip-flop design with a single logic stage which can include arbitrary logic functionality.

Working of DPSCRFF

The working of DPSCRFF depends on two stages**.**

1. Double pulse generator:

The two pulses are generated by a local pulse generator. The width of the pulses is controlled by the inverter delay chain and this inverter in the chain can be skewed to control the lengths of p1 and p2.the width of p2 determines the transparency window of latch. For designing any flip-flop setup and hold time should not be more. In DPSCRFF to reduce setup and hold time requirements p2 should be made as small as possible.

The conventional way to generate a pair of pulses uses an inverter delay chain as in figure 1.this design has large number of intermediate nodes and thus dissipate significant amount of power. Our alternative design reduces number of intermediate nodes by using an inverter delay chain both to generate p2 and to turn off p1.As shown in figure 2 intermediate node x is precharge high during the low phase of global clock. When the clock rises, p1 falls. After some delay p2 rises. This causes node x to discharge, causing p1 to rise. After some delay,p2 falls. Note that node x floats in the low state until the global clock goes low. This can be concern if the global clock is held high for a long time. In this design p1 and p2 overlap by some

amount. This cause some overlap current in the latch when the data input is high.

2. Operation of static latch:
The latch require two clock pulses,p1 and p2,which are generated from active clock edge. The first pulse preset the output node high using the p-type pull-up. The second pulse conditionally resets the output node, based on the value of the data input. The precharge causes the glitches at the output node whenever the output is supposed to remain low. An additional inverter can be added to the output stage to isolate the storage node from the output load.

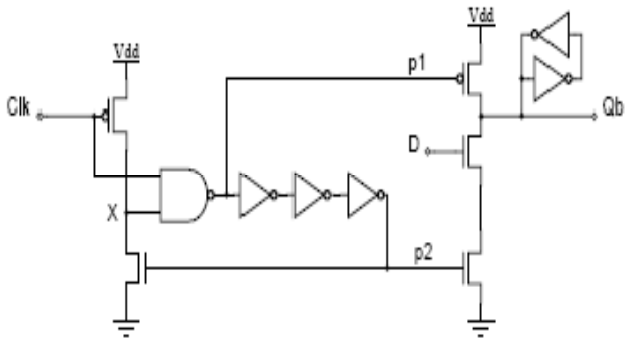

Figure 1 DPSCRFF

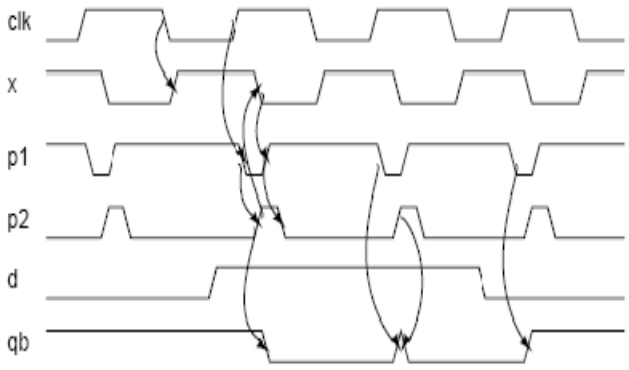

Figure 2 Operation of DPSCRFF

DPSCRFF Timing Analysis:
The DPSCRFF has asymmetric timing properties low input propagates through the flip flop in negative time as the output is preset at the start of p1. A low input must be set -up by the start of the second sampling pulse p2, and the hold time lasts for the duration of p2. A high input, however, can arrive later during the transparency period p2. The hold time of the high input just has to be large enough to switch the state of the static latch. The high value will still be correctly registered at the end of p2 even if the high value drops low again during p2. Fig.3 shows the two DPSCRFFs connected as a shift register to illustrate hold time violations. Consider the state just before a clock edge, when the first DPSCRFF had a reset value on Qb. This will be propagating through the combinational logic to the input of the second DPSCRFF.
At the clock edge, pulse p1 is generated and the first DPSCRFF will begin propagating a preset value from its output before the second DPSCRFF has sampled its input using pulse p2, potentially causing a hold time violation. A Conservative approach would be to require sufficient logic levels between DPSCRFFs such that the present value initiated by pulse p1 could not arrive at the second DPSCRFF until the end of pulse p2. If there are an odd number of inverting logic levels between the two DPSCRFFs, then the high-going preset value from the first DPSCRFF eventually propagates into a low-going value at the input to the second DPSCRFF. This low-going value will not cause a hold-time violation even if it arrives before the end of p2, provided that the previous input was high long enough to flip the latch state. In our technology, we found that five levels of FO4-loaded inverters between DPSCRFFs were sufficient to ensure no hold-time violations across PVT corners with ample margin (three levels just failed in one process corner). This DPSCRFF does not allow arbitrary time borrowing across the transparency window as with other pulsed latches.

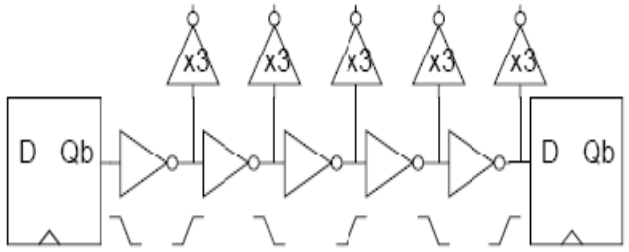

Figure 3 DPSCRFF shift register

DPSCRFF has a glitch in the case where the output Qb is to stay low, i.e., the input remained high. The precharge pulse p1 first forces the output high before the data input reset the output. This glitch can cause additional power dissipation in downstream logic. There is a tradeoff between the additional power dissipation caused by the glitch, and the possible power savings the glitch provides by enabling the use of highly skewed static logic. This is similar to the energy tradeoffs of precharged domino logic versus static logic.

III. PROBLEMS IN CONVENTIONAL DPSCRFF

There are some disadvantages in the DPSCRFF which make It slow and take large power during operation. Some problem is given below:

- This design has large number of intermediate node and thus dissipate significant amount of power.

- In this design, p1 and p2 overlap by some amount hence extra power caused by DPSCRFF.
- Large number of inverter in the pulse generator circuit for generation of pulse so large delay occurs.
- The output of the DPSCRFF has a glitch in the case where Qb is to stay low so this glitch cause additional power dissipation in the downstream logic.
- If the clock is running and data is held high, the DPSCRFF actually dissipates more power than for the full activity waveform because of its output glitches.

These disadvantages in the DPSCRFF can be amend by using proposed new flip flop called as double pulse latch flip -flop. In this flip flop the structure of pulse generator and MOS part is modified.

The modified design eliminates undesired glitches, extra Dynamic power which is caused by preset and static power. In block diagram the proposed new flip flop design is as below:

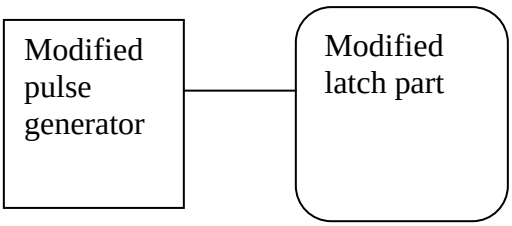

Figure 4 block diagram of proposed new flip-flop

IV. DOUBLE PULSE LATCH FLIP-FLOP

The DPLFF consist a static latch and pulse generator. Static latch required two pulses p1 and p2, which are generated from the active clock edge. When data in 0 PM2 is on and NM1 is off, the pulse p1 will be low for small amount of time with in that time output node will be charged. When the input data is '1' PM2 is off and NM1 is on pulse p2 will be high for small time and within that time output node will be discharged. In the Fig.6 operation of DPLFF is shown, whenever the output node is to be in low sate it remains low unlike DPSCRFF because of PM2 is off.

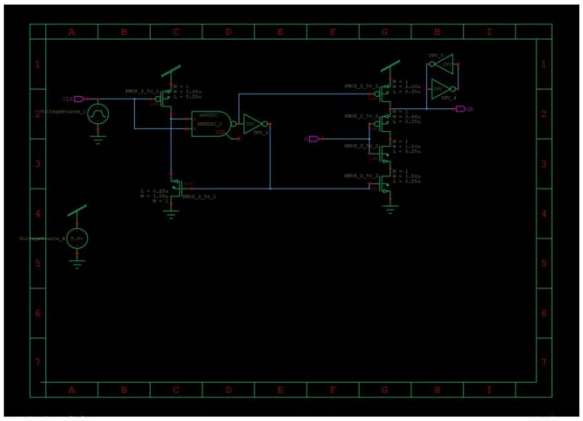

Figure 5 DPLFF using novel pulse generator

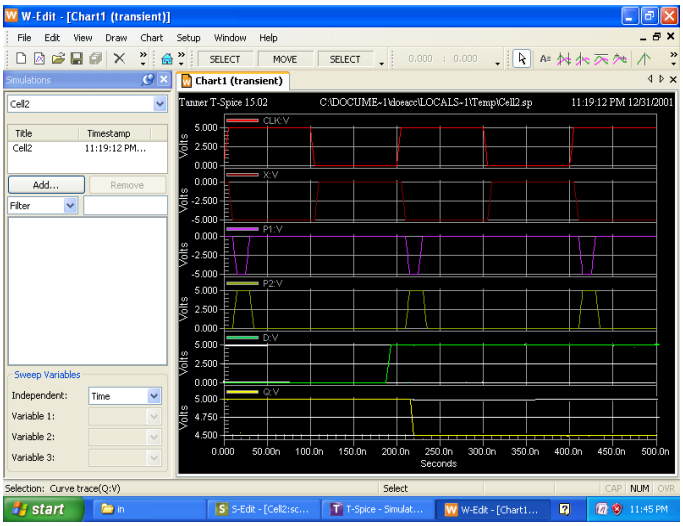

Figure 6 DLFF waveform

In pulse generator of DPLFF two invertors are removed after NAND gate. NMOS is switched on early than DPSCRFF because it is switched on after one inverter delay. By this way the width of pulses p1 and p2 is reduced, which reduces the transparence window of latch, which is desired.

Timing Analysis:

The DPLFF has symmetric properties pulse p1low and pulse p2 high almost at same time the input should not be changed during this time. But the width of the pulse p1 and p2 is less than that of the DPSCRFFs pulse p1 and p2.

In DPLFF NMOS in the clock generator is going to switch on after one inerter delay where as in conventional DPSCRFF after three inverter delay. This makes the DPLFF pulse (p1 and p2).

The propagation delay of required it the combinational circuit is also less than DPSCRFF. The maximum clock frequency also increases in the shift register when DPLFF is used.

Advantages of DPLFF over DPSCRFF:

- The first advantage in new double pulse latch flip is less number of inverter is used in pulse generator due to this delay reduced.
- The width of pulse is less in DPLFF due to less number of inverter and NMOS switched on early than DPSCRFF.
- The glitch is removed in DPFF because when Qb is to stay low the output is still low.
- The propagation delay of required in the combinational circuit is also less than DPSCRFF.

Evaluation and Simulation result:

I have simulated the circuit in Tanner software TSPICE 32 bit. The Schematic capture with S-Edit and Waveform viewing with W-Edit.

The power can be calculated by using formula:

$$P(t1, t2) = \frac{1}{t1}\int_{t1}^{t2} P(\tau)d\tau$$

Average power consumption DPSCRFF and DPLFF:

Average power consumed > 1.618804e-003 watts

Max power 2.311476e-003 at time 1e-009 and Min power 1.601938e-003 at time 5.225e-009.

Average power consumed > 8.005109e-005 watts

Max power 4.273679e-004 at time 1e-009 and Min power 7.941703e-005 at time 5e-009.

From the result it shows that DPLFF consumption is less compare to DPSCRFF.

Comparison of double pulse flip-flops:

Average power consumed in double pulse flip-flops	DPSCRFF	DPLFF
1.	1.618804e-003watt	8.005e-005watt

Delay	DPSCRFF	DPLFF
1.	35ns	25ns

Figure of Merrit	DPSCRFF	DLFF
1.	56 pico joule	200 pico joule

V. CONCLUSION

The modified DPFF has less power consumption compare to other fast flip-flop. The DPLFF pulse generator is modified this make the flip-flop fast. The DPLFF has the smallest D-to-Q delay with comparable to the lowest power flip-flop. The symmetric timing property makes it glitch free and this will reduce the power consumption. In serial operation as shift register DPLFF allows the higher frequency. The stacking of transistor in latch stage reduces sub threshold leakage current and thus the static power consumption is also less for DPLFF.

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