

COMPARE IMMEDIATE DATA WITH A REGISTER/MEMORY LOCATION

3.4 Compare immediate data with a Register/ Memory location

	Before	After
CMP BH, 0FH	BH <input type="text" value="56H"/>	<input type="text" value="56H"/>
56H=0101 0110B	AND	
	Temp <input type="text" value="45H"/>	<input type="text" value="47H"/>

CMP basically performs Subtract operation. Result of CMP is not stored in destination. It is stored in Temp register. Temp is not accessible to programmer. Only Flags are affected based result of subtraction.

3.4.1 Operand Instructions involving SR and R16/M16

	Before	After
MOV DS, CX	SR MOV <input type="text" value="1122H"/>	<input type="text" value="2233H"/>
	R16/M16	
	CX <input type="text" value="2233H"/>	

Note that there is no instruction to load an immediate data to a Segment register.

No. of opcodes = $2 \times 4 \times (8+24) = 256$

	Before	After	
MOV DS, [BX]	DS	1122H	2233H
	BX	2000H	
	DS:2000H	2233H	

3.4.2 Operand Instructions to perform Input operation

IN AL/AX, a8/DX 4 opcodes

	Before	After	
IN AL, DX	AL	50H	45H
	DX	2111H	
	Input port no. 2111H	45H	

	Before	After	
IN AL, 30H	AL	50H	45H
	Input port no. 30H	45H	

	Before	After	
IN AX, DX	AX	3050H	4045H
	DX	1177H	
	Input port no. 60H	45H	
	Input port no. 61H	40H	

3.4.3 Operand Instructions to perform Output operation

OUT a8/DX, AL/AX 4 opcodes

	Before	After	
OUT 30H, AL	AL	50H	
	Out port no. 30H	40H	50H

	Before	After		
OUT DX, AX	AX	3050H	50H	
	DX	2177H		
	Out port no. 2177H	45H		30H
	Out port no. 2178H	40H		

	Before	After	
OUT 60H, AX	AX	3050H	_____

Out port no. 60H	45H	50H
Out port no. 61H	40H	30H

3.4.4 Operand Instructions to perform Shift/Rotate operation

ROR /ROL /RCR /RCL /SHR /SHL /SAR R/M, 1/CL

7 instructions x (16+48) x 2 = 896 opcodes

SHR and SHL: for shifting left / right unsigned numbers

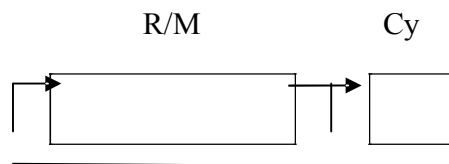
SAR used Shifting right a signed number

SHL is also called as SAL, as method for shift left of signed or unsigned number is the same

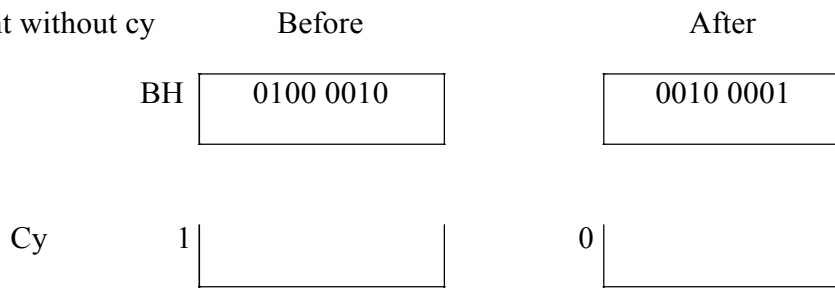
ROR R/M, 1/CL Used for division by power of 2

CL has no. of times rotation is to be done

ROR BH, 1



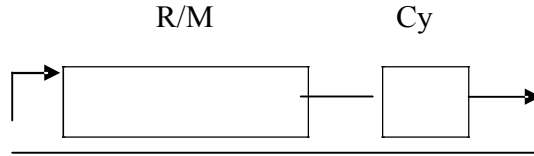
Rotate right without cy



RCR R/M, 1/CL

CL has no. of times rotation is to be done

RCR BH, 1



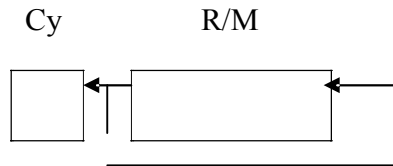
Rotate right with cy

	Before	After
BH	0100 0010	1010 0001
Cy	1	0

ROL R/M, 1/CL

Used for multiplication by 2^n

ROL BH, CL

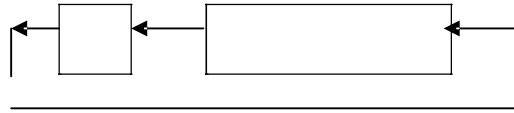


Rotate left without cy

	<i>Before</i>	<i>After</i>
BH	0010 0010	1000 1000
CL	02H	
Cy	1	0

RCL R/M, 1/CL

RCL BH, CL Cy R/M



Rotate left with cy

	<i>Before</i>	<i>After</i>
BH	0010 0010	1000 0010
CL	02H	
Cy	1	0

SHL R/M, 1/CL

Used for multiplication by 2^n

SHL BH, CL Cy R/M



Shift left without cy

	<i>Before</i>	<i>After</i>
BH	0010 0010	1000 1000
CL	02H	
Cy	1	0

SHR R/M, 1/CL

Used for division by 2^n of unsigned nos

SHR BH, CL R/M Cy



Shift right

	<i>Before</i>	<i>After</i>
BH	0100 0100	0001 0001
CL	02H	
Cy	1	0

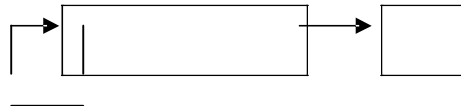
SAR R/M, 1/CL

Used for division by 2^n of signed nos

SAR BH, CL

R/M

Cy



Shift right

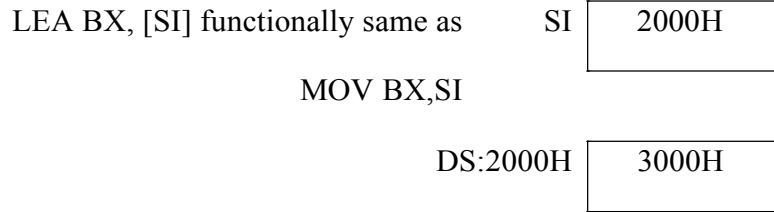
	<i>Before</i>	<i>After</i>
1100 0000 = -40H	BH 1100 0000	1111 0000
1111 0000 = -10H	CL 02H	
	Cy 1	0

3.4.5 Operand instruction to load an Effective address into an Address Register

LEA AR, a16

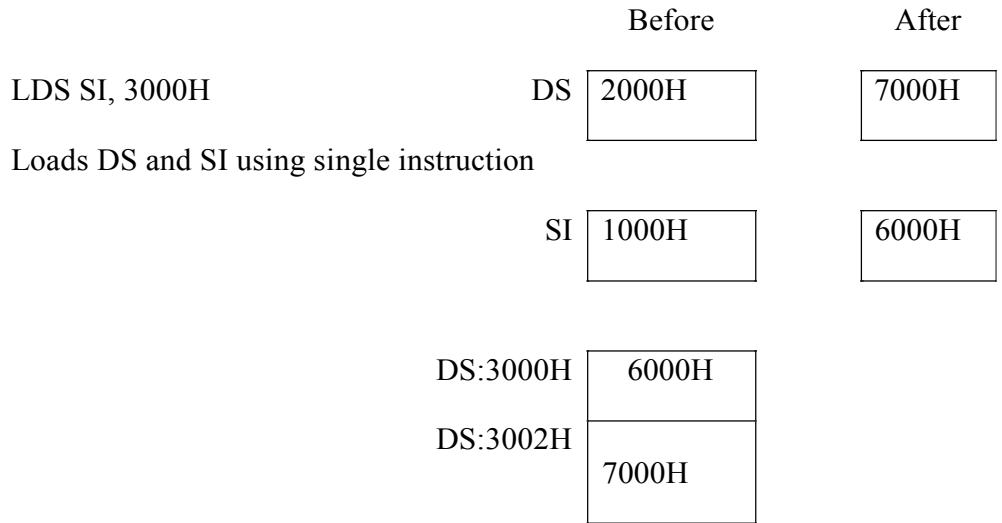
4 x 24 = 96 opcodes

		Before	After
LEA BX, [SI]	BX	1000H	2000H



3.4.6 Operand instruction to load DS and an Address Register from memory

LDS AR, M32 $4 \times 24 = 96$ opcodes



3.4.7 Operand instruction to load ES and an Address Register from memory

LES AR, M32 $4 \times 24 = 96$ opcodes

		Before	After
LES DI, 3000H	ES	2000H	7000H
Loads ES and DI using single instruction	DI	1000H	6000H
	2000:3000H	6000H	
	2000:3002H	7000H	

Source : <http://elearningatria.files.wordpress.com/2013/10/cse-iv-microprocessors-10cs45-notes.pdf>