CMOS LOGIC - AN INTRODUCTION

The various applications that require logic structures have different optimizations. Some of the circuit needs fast response, some slow but very precise response; others may need large functionality in a small space and so on. The CMOS logic structures can be implemented in alternate ways to get specific optimization. These optimizations are specific because of the tradeoff between the n numbers of design parameters.

CMOS COMPLEMENTARY LOGIC

CMOS logic structures of nand & nor has been studied in previous unit. They were ratioed logic i.e. they have fixed ratio of sizes for the n and the p gates. It is possible to have ratio less logic by varying the ratio of sizes which is useful in gate arrays and sea of gates. Variable ratios allow us to vary the threshold and speed .If all the gates are of the same size the circuit is likely to function more correctly. Apart from this the supply voltage can be increased to get better noise immunity. The increase in voltage must be done within a safety margin of the source -drain break down. Supply voltage can be decreased for reduced power dissipation and also meet the constraints of the supply voltage. Sometimes even power down with low power dissipation is required. For all these needs an on chip voltage regulator is required which may call for additional space requirement. A CMOS requires a nblock and a pblock for completion of the logic. That is for a n input logic 2n gates are required. The variations to this circuit can include the following techniques reduction of noise margins and reducing the function determining transistors to one polarity.

BICMOS Logic

The CMOS logic structures have low output drive capability. If bipolar transistors are used at the output the capability can be enhanced. Bipolar transistors are current controlled devices and produces larger output current then the CMOS transistors. This combined logic is called BICMOS logic. We can have the bipolar transistors both for pull up and pull down or only for pull up as shown in the figures below. The figure next shows a CMOS nand gate with NPN transistors at both levels. The Nl & N2 supply current to the base of the NPN2 transistor when the output is high and hence the it can pull it down with larger speed. When the output is low N3 clamps the base current to NPN2, Pl & P2 supply the base current to NPNl

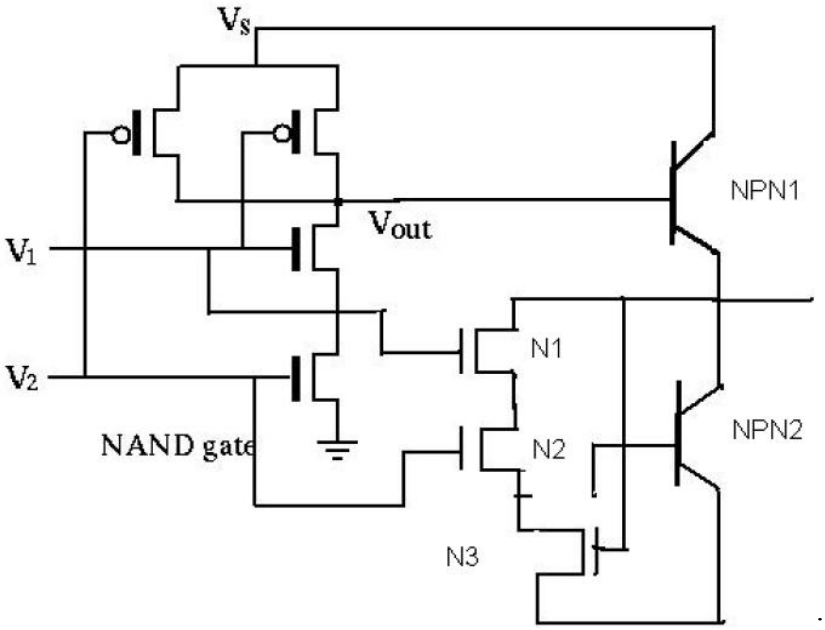

Figure 1: Nand with two NPN drivers

This design shown previously is basically used for speed enhancing in highly automated designs like gate arrays. Since the area occupied by the Bipolar transistors is more and if the aim in the design is to match the pull up and pull down speeds then we can have a transistor only in the pull up circuit because p devices are slower as shown in the figure next. The usage of BiCMOS must be done only after a trade off is made between the cost, performance etc.

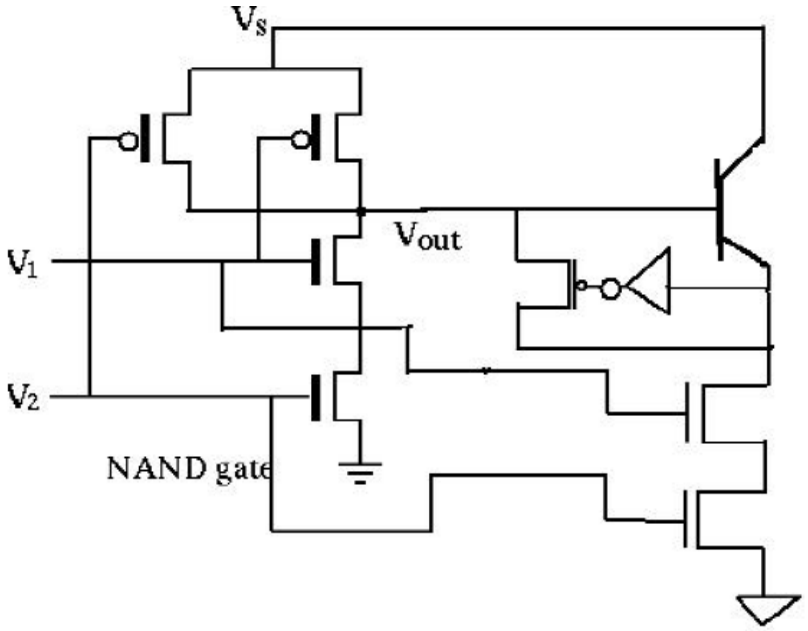

Figure 2: Nand with one NPN in pull up.

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