CMOS INVERTER CHARACTERISTICS

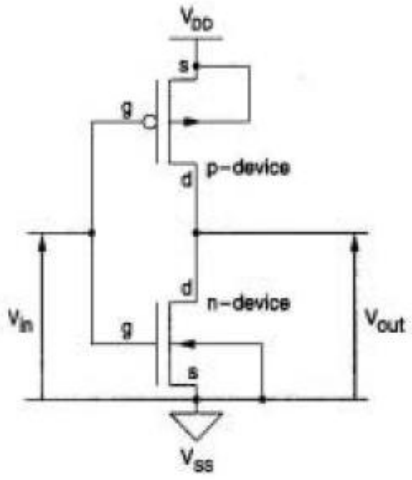

Figure 20: CMOS Inverter

CMOS inverters (Complementary NOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large.

A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, were VIN is connected to the gate terminals and VOUT is connected to the drain terminals.(given in diagram). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and VDD, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter's operations can be seen very easily:

MOSFET	Condition on MOSFET	State of MOSFET
NMOS	Vgs<Vtn	OFF
NMOS	Vgs>Vtn	ON
PMOS	Vsg<Vtp	OFF
PMOS	Vsg>Vtp	ON

The table given, explains when the each transistor is turning on and off. When VIN is low, the NMOS is "off", while the PMOS stays "on": instantly charging VOUT to logic high. When Vin is high, the NMOS is "on and the PMOS is "off": taking the voltage at VOUT to logic low.

1.10.1 Inverter DC Characteristics:

Before we study the DC characteristics of the inverter we should examine the ideal characteristics of inverter which is shown below. The characteristic shows that when input is zero output will high and vice versa.

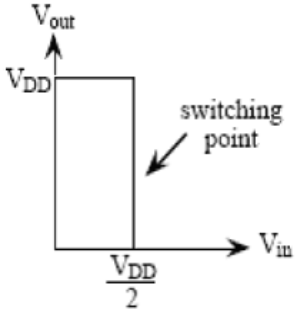

Figure 21: Ideal Characteristics of an Inverter.

The actual characteristic is also given here for the reference. Here we have shown the status of both NMOS and PMOS transistor in all the regions of the characteristics.

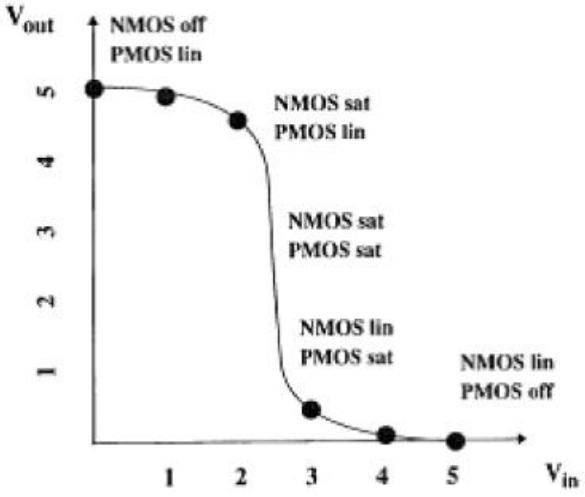

Figure 22: Actual Characteristics of an Inverter.

Graphical Derivation of Inverter DC Characteristics:

The actual characteristics are drawn by plotting the values of output voltage for different values of the input voltage. We can also draw the characteristics, starting with the VI characteristics of PMOS and NMOS characteristics.

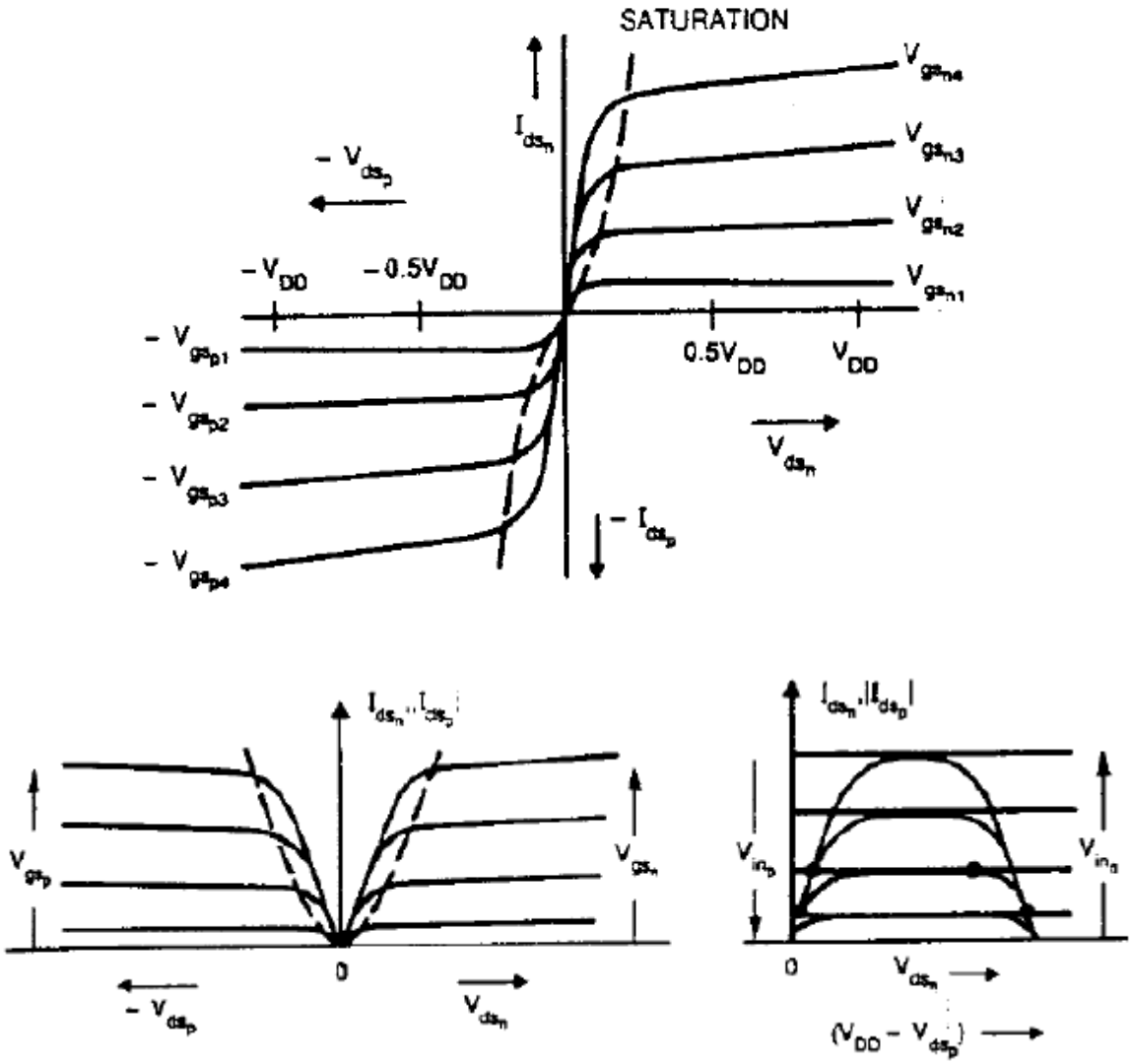

Figure 23-a,b,c: Graphical Derivation of DC Characteristics.

The characteristics given in figure 23a is the vi characteristics of the NMOS and PMOS characteristics (plot of Id vs. Vds). The figure 23b shows the values of drain current of PMOS transistor is taken to the positive side the current axis. This is done by taking the absolute value of the current. By superimposing both characteristics it leads to figure 23c. the actual characteristics may be now determined by the points of common Vgs intersection as shown in figure 23d.

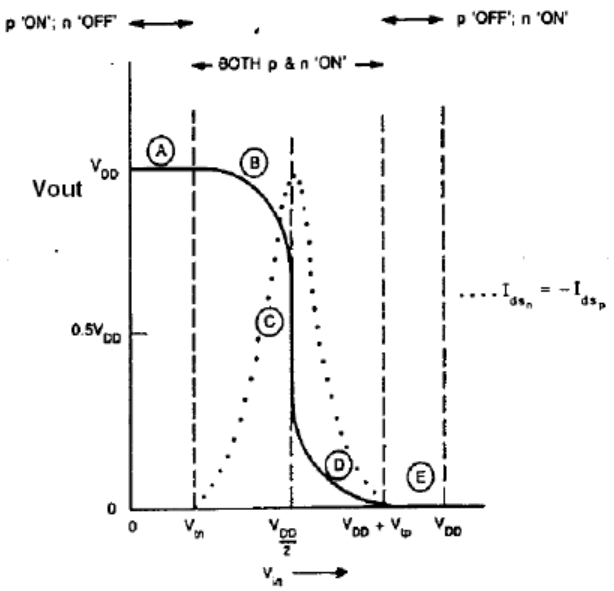

Figure 23d: CMOS Inverter Dc Characteristics.

Figure 23d shows five regions namely region A, B, C, D & E. also we have shown a dotted curve which is the current that is drawn by the inverter.

Region A:

The output in this region is high because the P device is OFF and n device is ON. In region A, NMOS is cutoff region and PMOS is on, therefore output is logic high. We can analyze the inverter when it is in region B. the analysis is given below:

Region B:

The equivalent circuit of the inverter when it is region B is given below.

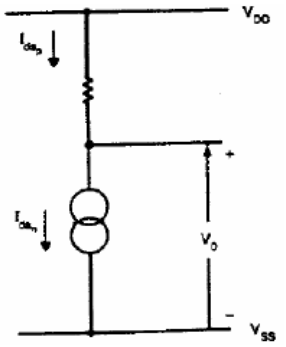

Figure 24: Equivalent circuit in Region B.

In this region PMOS will be in linear region and NMOS is in saturation region.

The expression for the NMOS current is

$$I_{ds_n} = \beta_n \frac{[V_{in} - V_{t_n}]^2}{2},$$

The expression for the PMOS current is

$$I_{ds_p} = -\beta_p \left[(V_{in} - V_{DD} - V_{t_p})(V_O - V_{DD}) - \frac{1}{2}(V_O - V_{DD})^2 \right]$$

The expression for the voltage Vo can be written as

$$V_O = (V_{in} - V_{t_p}) + \left[(V_{in} - V_{t_n})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{t_p} \right) V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{t_n})^2 \right]^{1/2}$$

Region C:

The equivalent circuit of CMOS inverter when it is in region C is given here. Both n and p transistors are in saturation region, we can equate both the currents and we can obtain the expression for the midpoint voltage or switching point voltage of a inverter. The corresponding equations are as follows:

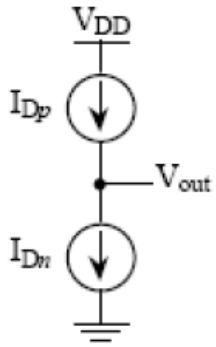

Figure 25: Equivalent circuit in Region C.

The corresponding equations are as follows:

$$I_{ds_p} = \frac{1}{2}\beta_p (V_{in} - V_{DD} - V_{t_p})^2$$

$$I_{ds_n} = \frac{1}{2}\beta_n (V_{in} - V_{t_n})^2$$

By equating both the currents, we can obtain the expression for the switching point voltage as,

$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Region D: The equivalent circuit for region D is given in the figure below.

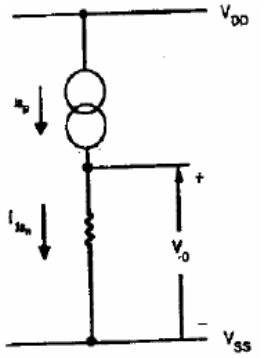

Figure 26: equivalent circuit in region D.

We can apply the same analysis what we did for region B and C and we can obtain the expression for output voltage.

Region E:

The output in this region is zero because the P device is OFF and n device is ON.

Influence of βn / βp on the VTC characteristics:

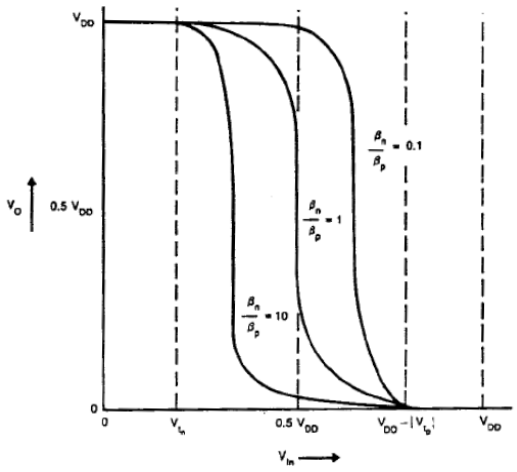

Figure 27: Effect of βn/βp ratio change on the DC characteristics of CMOS inverter.

The characteristics shifts left if the ratio of βn/βp is greater than 1(say 10). The curve shifts right if the ratio of βn/βp is lesser than 1(say 0.1). This is decided by the switching point equation of region C. the equation is repeated here the reference again.

$$Vm=Vsp=V_{DD}+Vtp+Vtn(\beta n/\beta p)1/2 \,/\, 1+(\beta n/\beta p)1/2$$

Noise Margin:

Noise margin is a parameter related to input output characteristics. It determines the allowable noise voltage on the input so that the output is not affected. We will specify it in terms of two things:

- LOW noise margin
- HIGH noise margin

LOW noise margin: is defined as the difference in magnitude between the maximum Low output voltage of the driving gate and the maximum input Low voltage recognized by the driven gate.

$$\mathbf{NML=|VILmax - VOLmax|}$$

HIGH noise margin: is defined difference in magnitude between minimum High output voltage of the driving gate and minimum input High voltage recognized by the receiving gate.

$$\mathbf{NMH=|Vohmin - VIHmin|}$$

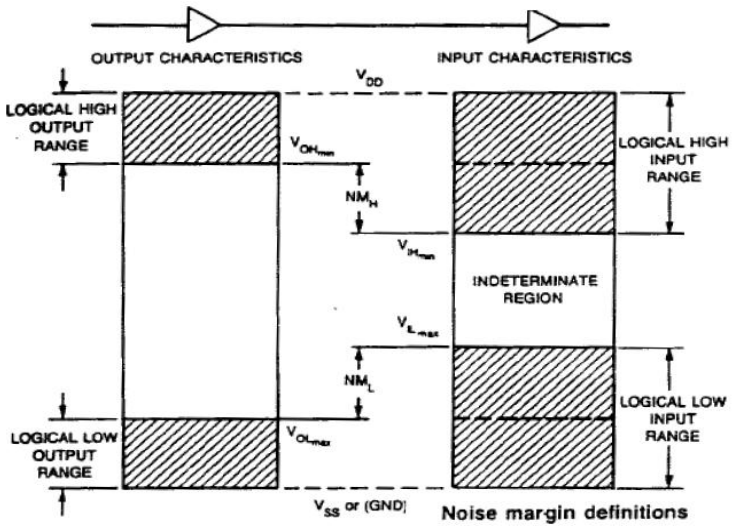

Figure 28: noise margin definitions.

Figure shows how exactly we can find the noise margin for the input and output. We can also find the noise margin of a CMOS inverter. The following figure gives the idea of calculating the noise margin.

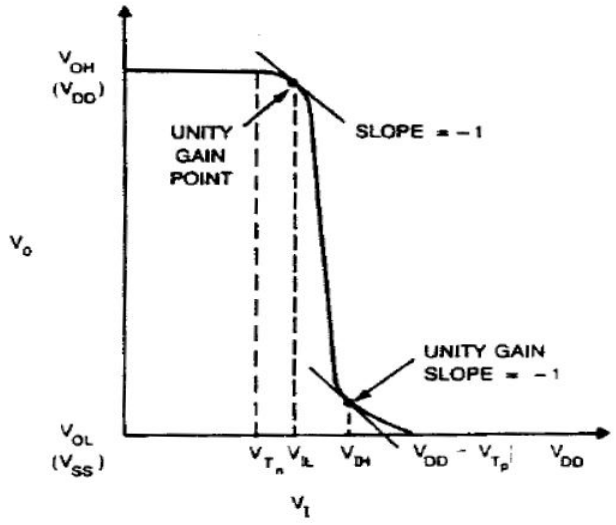

Figure 29: CMOS inverter noise margins.

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