CMOS FABRICATION CAN BE ACCOMPLISHED USING EITHER OF THE THREE TECHNOLOGIES

- N-well/P-well technologies
- Twin well technology
- Silicon On Insulator (SOI)

Twin Well Technology

Using twin well technology, we can optimise NMOS and PMOS transistors separately. This means that transistor parameters such as threshold voltage, body effect and the channel transconductance of both types of transistors can be tuned independently.
n+ or p+ substrate, with a lightly doped epitaxal layer on top, forms the starting material for this technology. The n-well and p-well are formed on this epitaxial layer which forms the actual substrate. The dopant concentrations can be carefully optimized to produce the desired device characterisitcs because two independent doping steps are performed to create the well regions.

The conventional n-well CMOS process suffers from, among other effects, the problem of unbalanced drain parasitics since the doping density of the well region typically being about one order of magnitude higher than the substrate. This problem is absent in the twin-tub process.

Silicon on Insulator (SOI)

To improve process characteristics such as speed and latch-up susceptibility, technologists have sought to use an insulating substrate instead of silicon as the substrate material.
Completely isolated NMOS and PMOS transistors can be created virtually side by side on an insulating substrate (eg. sapphire) by using the SOI CMOS technology.
This technology offers advantages in the form of higher integration density (because of the absence of well regions), complete avoidance of the latch-up problem, and lower parasitic capacitances compared to the conventional n-well or twin-tub CMOS processes.
But this technology comes with the disadvantage of higher cost than the standard n-well CMOS process. Yet the improvements of device performance and the absence of latch-up problems can justify its use,especially in deep submicron devices.

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N-well Technology

In this discussion we will concentrate on the well established n-well CMOS fabrication technology, which requires that both n-channel and p-channel transistors be built on the same chip substrate. To accomodate this, special regions are created with a semiconductor type opposite to the substrate type. The regions thus formed are called wells or tubs. In an n-type substrate, we can create a p-well or alternatively, an n-well is created in a p-type substrate. We present here a simple n-well CMOS fabrication technology, in which the NMOS transistor is created in the p-type substrate, and the PMOS in the n-well, which is built-in into the p-type substrate.

Historically, fabrication started with p-well technology but now it has been completely shifted to n-well technology. The main reason for this is that, "n-well sheet resistance can be made lower than p-well sheet resistance" (electrons are more mobile than holes).

The simplified process sequence for the fabrication of CMOS integrated circuits on a p-type silicon substrate is as follows:

- N-well regions are created for PMOS transistors, by impurity implantation into the substrate
- This is followed by the growth of a thick oxide in the regions surround the NMOS and PMOS active regions.
- The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- After this n+ and p+ regions (source, drain and channel-stop implants) are created.
- The metallization step (creation of metal interconnects) forms the final step in this process

The integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide, since each processing step requires that certain areas are defined on chip by appropriate masks. A layer is patterned before the next layer of material is applied on the chip. A process, called lithography, is used to transfer a pattern to a layer. This

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must be repeated for every layer, using a different mask, since each layer has its own distinct requirements.

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