

# BASIC CIRCUIT CONCEPTS - AN INTRODUCTION

We have already seen that MOS structures are formed by the super imposition of a number conducting, insulating and transistor forming material. Now each of these layers have their own characteristics like capacitance and resistances. These fundamental components are required to estimate the performance of the system. These layers also have inductance characteristics that are important for I/O behavior but are usually neglected for on chip devices.

The issues of prominence are

1. Resistance, capacitance and inductance calculations.
2. Delay estimations
3. Determination of conductor size for power and clock distribution
4. Power consumption
5. Charge sharing
6. Design margin
7. Reliability
8. Effects and extent of scaling

## 4.2 RESISTANCE ESTIMATION

The concept of sheet resistance is being used to know the resistive behavior of the layers that go into formation of the MOS device. Let us consider a uniform slab of conducting material of the following characteristics.

Resistivity- $\rho$

Width -  $W$

Thickness -  $t$

Length between faces –  $L$  as shown next

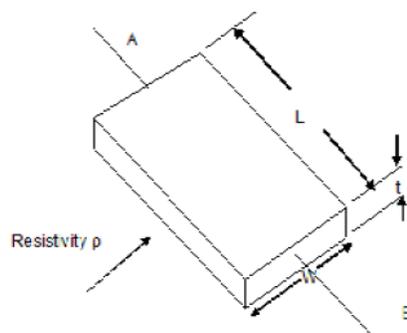


Figure 1: A slab of semiconductor.

We know that the resistance is given by  $R_{AB} = \rho L/A \Omega$ . The area of the slab considered above is given by  $A=Wt$ . Therefore  $R_{AB} = \rho L/Wt \Omega$ . If the slab is considered as a square then  $L=W$ . therefore  $R_{AB} = \rho /t$  which is called as sheet resistance represented by  $R_s$ . The unit of sheet resistance is **ohm per square**. It is to be noted that  $R_s$  is independent of the area of the slab. Hence we can conclude that a 1um per side square has the same resistance as that of 1cm per side square of the same material. The resistances of the different materials that go into making of the MOS device depend on the resistivity and the thickness of the material. For a diffusion layer the depth defines the thickness and the impurity defines the resistivity. The table of values for a 5u technology is listed below. 5u technology means minimum line width is 5u and  $\lambda = 2.5u$ . The diffusion mentioned in the table is n diffusion, p diffusion values are 2.5 times of that of n. The table of standard sheet resistance value follows.

Layer	$R_s$ per square
Metal	0.03
Diffusion n(for 2.5 times the n )	10 to 50
Silicide	2 to 4
Polysilicon	15 to 100
N transistor gate	$10^4$
P transistor gate	$2.5 \times 10^4$

#### SHEET RESISTANCE OF MOS TRANSISTORS

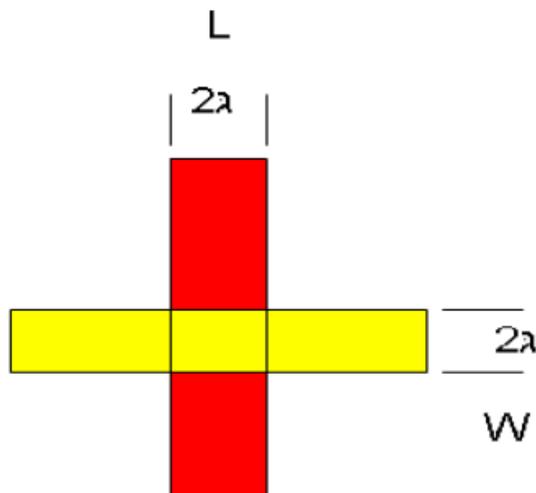


Figure 2: Min sized inverter.

The N transistor above is formed by a  $2a$  wide poly and n diffusion. The L/W ratio is 1. Hence the transistor is a square, therefore the resistance R is  $1 \times R_s$  ohm/sq i.e.  $R = 1 \times 10^4$ . If L/W ratio is 4 then  $R = 4 \times 10^4$ . If it is a P transistor then for L/W = 1, the value of R is  $2.5 \times 10^4$ .

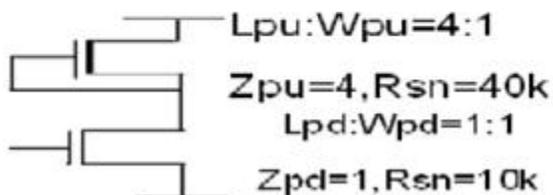


Figure 3: Nmos depletion inverter.

Pull up to pull down ratio = 4. In this case when the nmos is on, both the devices are on simultaneously, Hence there is an on resistance  $R_{on} = 40 + 10 = 50k$ . It is this resistance that leads the static power consumption which is the disadvantage of nmos depletion mode devices

INVERTER RESISTANCE CALCULATION

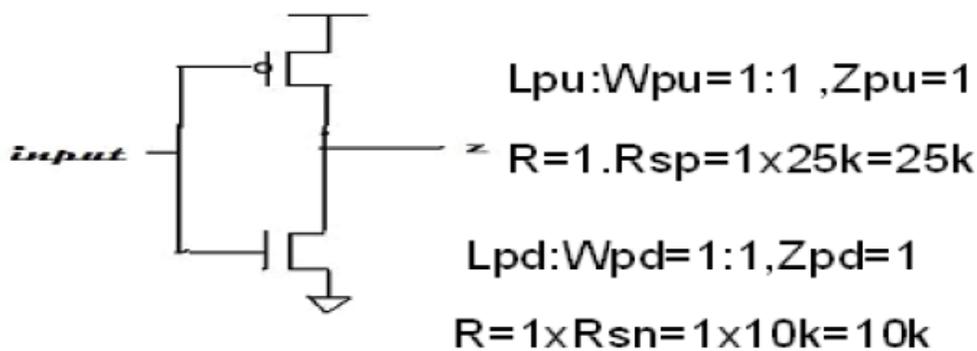


Figure 4: CMOS inverter.

Since both the devices are not on simultaneously there is no static power dissipation. The resistance of non-rectangular shapes is a little tedious to estimate. Hence it is easier to convert the irregular shape into regular rectangular or square blocks and then estimate the resistance. For example

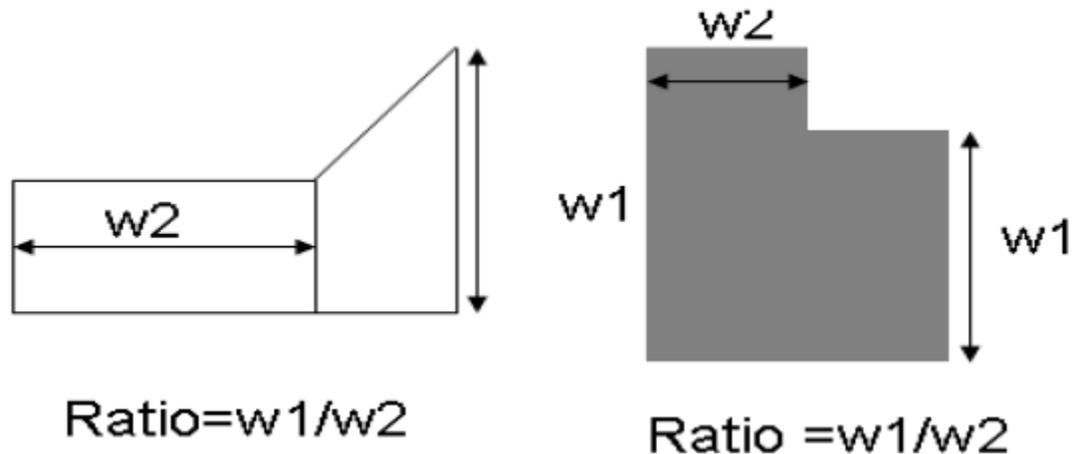


Figure 5: Irregular rectangular shapes.

#### CONTACT AND VIA RESISTANCE

The contacts and the vias also have resistances that depend on the contacted materials and the area of contact. As the contact sizes are reduced for scaling, the associated resistance increases. The resistances are reduced by making ohmic contacts which are also called loss less contacts. Currently the values of resistances vary from .25ohms to a few tens of ohms.

#### SILICIDES

The connecting lines that run from one circuit to the other have to be optimized. For this reason the width is reduced considerably. With the reduction in width the sheet resistance increases, increasing the RC delay component. With polysilicon the sheet resistance values vary from 15 to 100 ohm. This actually affects the extent of scaling down process. Polysilicon is being replaced with silicide. Silicide is obtained by depositing metal on polysilicon and then sintering it. Silicides give a sheet resistance of 2 to 4 ohm. The reduced sheet resistance makes silicides a very attractive replacement for polysilicon. But the extra processing steps is an offset to the advantage.