## AN NMOS INVERTER

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. The truth table is shown on the right.

This represents *perfect* switching behavior, which is the defining assumption in Digital electronics. In practice, actual devices have electrical characteristics that must be carefully considered when designing inverters. In fact, the non-ideal *transition region* behavior of a CMOS inverter makes it useful in analog electronics as a class A amplifier (e.g., as the output stage of an operational amplifier)

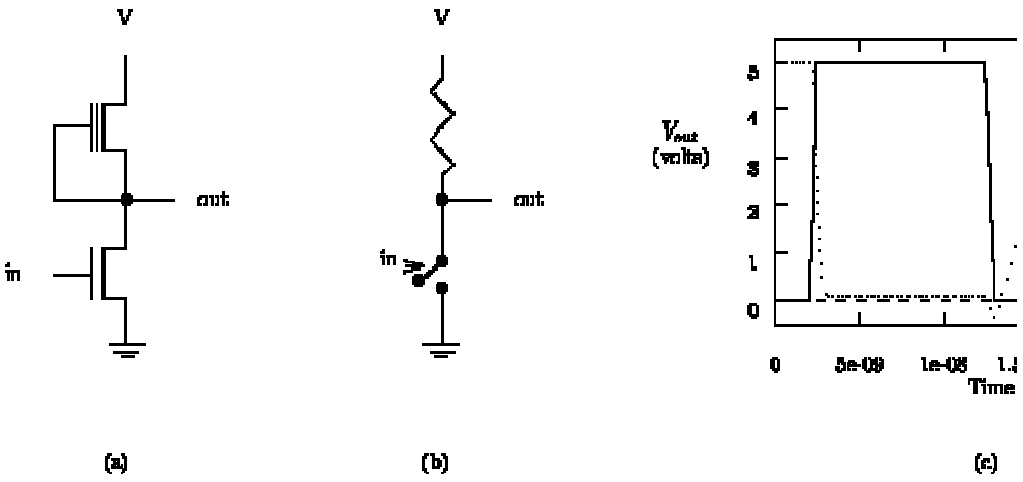



**Figure: 4** An NMOS inverter

The gate of the depletion mode transistor is connected to its drain, to keep the transistor permanently turned on. The depletion mode transistor is used as a ``pull-up" resistor, and the enhancement mode transistor is used as a switch to ``pull down" the output when the switch is turned on. Note that in this technology, the resistance of the permanently turned on depletion mode transistor must be large compared with the ``on" resistance of the enhancement mode transistor, but small compared with the ``off" resistance of the transistor. This type of logic is often called a ``ratioed logic", since the ratio of the pull-up resistance to the pull-down resistance effectively determines the voltage at which the output of the device changes state. Typically, $R_{pu} \approx 4R_{pd}$. The large resistive pull-up transistor causes three particular problems with this technology:

1. The depletion mode transistor must be made large ( *i.e.*, long and thin) to create the large ``on" resistance.

2. When driving a capacitive output load such as the gate of another transistor, the charging time (proportional to $R_{dep}C$) will be long compared to the discharging time (proportional to $R_{enh}C$). This effect is clearly evident in Figure 2.7 (c).
3. The device consumes DC power whenever the enhancement mode pull down device is turned on, due to the resistive losses in the pull-up transistor.

The third problem becomes more serious as feature sizes for transistors decrease, because the number of such resistors per unit area increases, and the devices may not dissipate the heat as well, resulting in device failure due to overheating.

## Pull up to Pull-down ratio for a NMOS Inverter and CMOS Inverter (Bn/Bp)

- Inverter : basic requirement for producing a complete range of Logic circuits

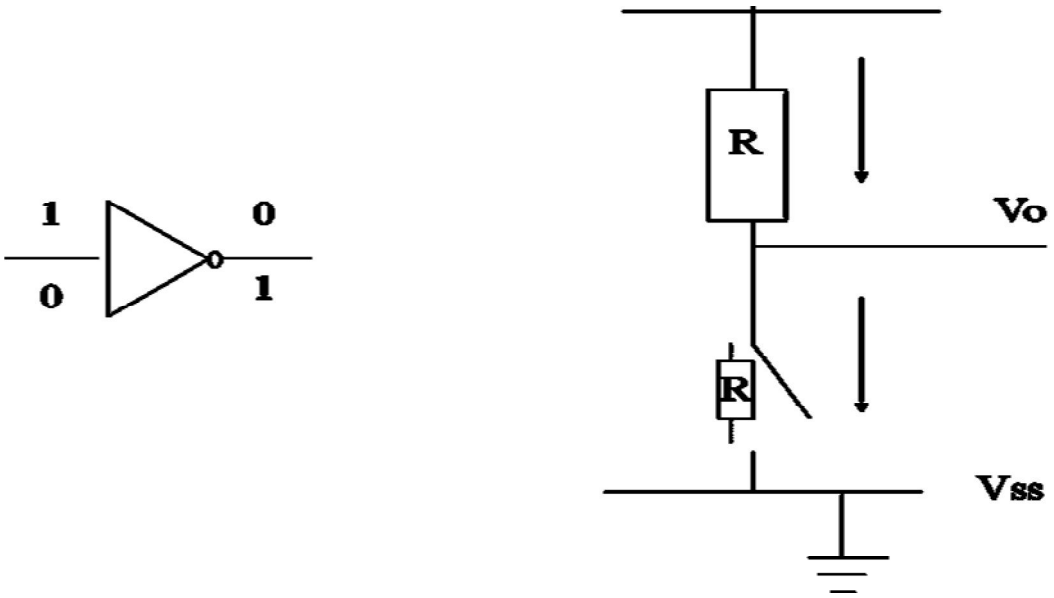



**Fig. 5 Inverter**

Basic Inverter: Transistor with source connected to ground and a load resistor connected from the drain to the positive Supply rail Output is taken from the drain and control input connected

between gate and ground Resistors are not easily formed in silicon they occupy too much area Transistors can be used as the pull-up device.

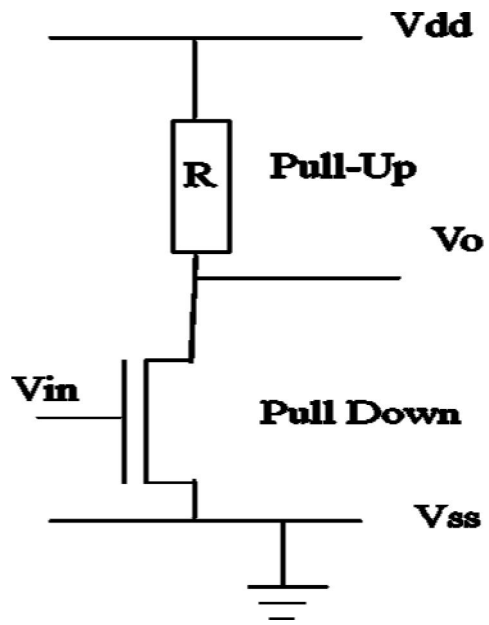
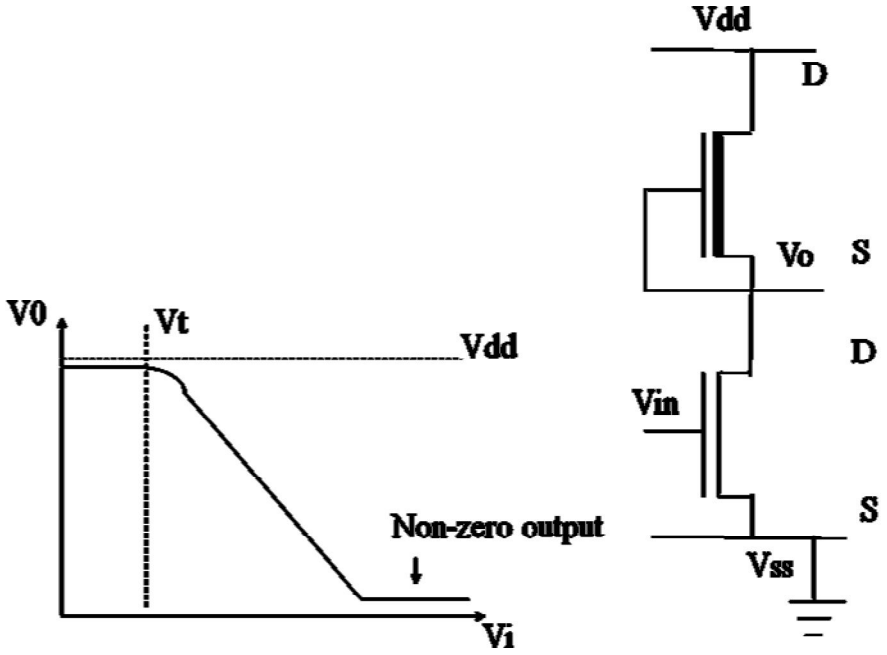
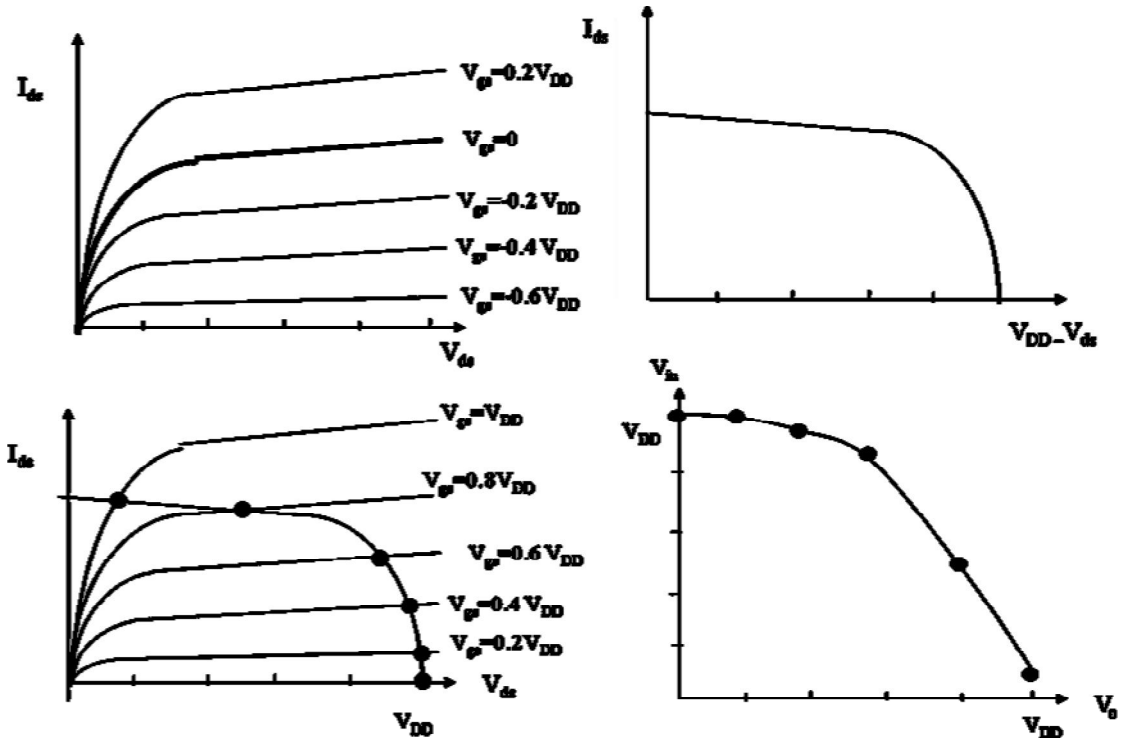



**Fig. 6 Pull UP & Pull down Network**

- NMOS Depletion Mode Transistor Pull - Up Pull-Up is always on – Vgs = 0; depletion Pull-Down turns on when Vin > Vt With no current drawn from outputs, Ids for both transistors is equal


Vdd
D
Vo
S
D
Vin
S
Vss
V0
Vt
Vdd
Non-zero output
Vi


$I_{ds}$
$V_{gs}$=0.2$V_{DD}$
$V_{gs}$=0
$V_{gs}$=-0.2 $V_{DD}$
$V_{gs}$=-0.4 $V_{DD}$
$V_{gs}$=-0.6$V_{DD}$
$V_{ds}$
$I_{ds}$
$V_{DD}$-$V_{ds}$
$I_{ds}$
$V_{gs}$=$V_{DD}$
$V_{gs}$=0.8$V_{DD}$
$V_{gs}$=0.6 $V_{DD}$
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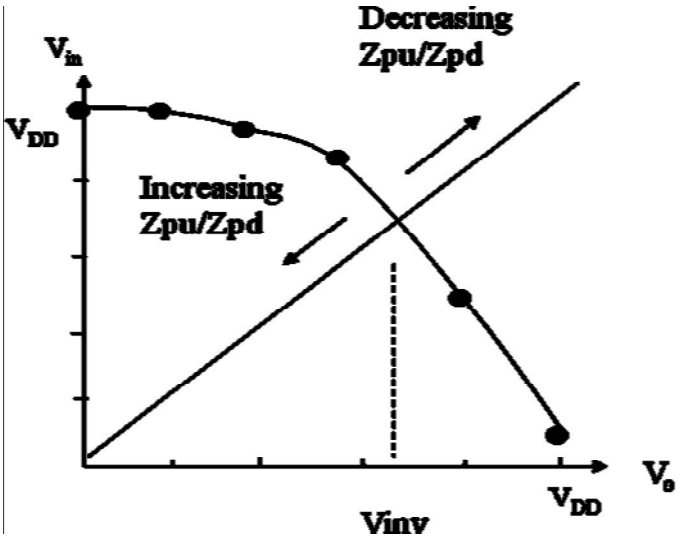


**Fig. 7 Characteristics of MOS**

Point where Vo = Vin is called Vinv

Transfer Characteristics and Vinv can be shifted by altering ratio of pull-up to Pull down impedances

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