A FULLY INTEGRATED NEURAL SIGNAL ACQUISITION AMPLIFIER FOR EPILEPTIC SEIZURE PREDICTION

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Abstract - This paper deals with the design of low power low noise neural signal amplifier for Epileptic Seizure Prediction. The advent of Micro-electro Arrays has driven the need for implantable electronic circuitry to detect those Extracellular neural signals (ENG). We proposed a preamplifier of fully differential Low Noise Amplifier (LNA) with gm boosting in order to enhance the gain as well as reduce the power consumption. Low frequency high pass function has been realized with anti-parallel Diode connected PMOS. Simulation results shows that the input referred noise is 1.24µVrms from 100Hz to 5 KHz, mid-band voltage gain of 44.6dB, and the power consumption is 18.74µw. A new signal processing circuit has been designed extract the seizure onset. The results are validated using Cadence spectre simulator with 180nm technology. Simulation results show that this implantable amplifier is suitable for Epileptic seizure prediction.

Keywords: Epileptic Seizure, NSA, pseudo resistor, Low frequency High Pass Function (LFHPF)

I. INTRODUCTION

Early prediction of severe epilepsy may helpful for the patients to escape from fatal accidents. Much research is being done on Epileptic seizure prediction using EEG Signals. While using EEG signals many false positives are reported. So, the better alternate for this system is to use implantable devices recording ENG signals. ENG signals are small in amplitude from 5µV to 500µV and have a low frequency spectrum of 100Hz to 5 KHz[1]. However in practice, the distance of Micro-electrode arrays (MEA) are difficult to control and the resulting ENG is very small requiring a LNA for signal amplification cum detection.

The overall block diagram for Epileptic Seizure detection is shown in figure1. Output from the ENG signal acquisition amplifier (NSA) is directly taken as clinical data, further the signal is sent through a proposed simple signal processor to extract the seizure onset. Later the extracted feature will be compared with the reference neural signal Potential (Vsyn) using high speed latch comparator.[2] The composite Neural signal consists of large DC offset due to the body fluid where the MEA resides and Electromyography (EMG) noise, Power Line frequency interference. The DC offset and EMG noise can be removed by Low frequency High Pass Function [3].

MOSFET based design for low frequency biomedical application has inherent flicker noise, it cause poor SNR. Some of the solutions to reduce the flicker noise are chopper stabilization and Auto-zeroing, both cases consumes more power, it is not advisable for implantable applications [4,5]. The flicker noise is dominating in the PMOS. The flicker noise and the valid signals are having the same 150Hz spectrum, so the transistors made large to increase its transconductance (gm) [6], thereby the noise is eliminated. The proposed LNA with sub-threshold PMOS input pair with gm- boosting shows valid results.

![Figure 1. Overall Block Diagram of Epileptic Seizure Detection](image-url)

This LNA has fully differential topology in order to eliminate the coherent noise. The design of low frequency High pass function is challenging one. In our proposed Circuit Anti-parallel Diode connected PMOS is used as Pseudo resistor. It consumes less power and exhibits bilinear characteristics. The differential output is converted into single ended by the high linear OTA-C filter, which is nothing but a Low pass Filter in this design[6].

The section1 gives brief Introduction of this Work, section II explain the inductively coupled power supply for implantable circuits, section III explains the realization of Pseudo-resistors, section IV describes the functionality of low frequency high pass function, section V explains the functional details of LNA, Section VI reveals the LNA Noise Analysis, Section VII explains about the High Linear Low Pass filter, section VIII explains a new signal processing circuit and Section IX Concludes the work with the obtained parameters.
II INDUCTIVE COUPLED RAIL-TO-RAIL SUPPLY

For the past few years, high-performance implantable bio-medical ICs plays a major role in modern medicine. With the advent of nanotechnology, Battery based circuits are not entertained for implantable applications. Nowadays, inductively coupled link is more desirable method for patient, because of its high power transfer efficiency and safety. Bio-medical amplifiers shows good result, when using rail-to-rail power supply. In the proposed method, the sinusoidal output from the secondary coil is applied between the terminals X and Y. When potential on side X is more than that of Y, the transistors Mb,Mc,Mf and Mg are forced to shut-off while Ma,Md,Me and Mh are turned on. Therefore, we can get positively and negatively unidirected supply from terminals +Vr and −Vr respectively for both positive and negative half cycles. The unidirected supply is passed through a capacitor filter to remove its ac contents (ripples). By using a suitable regulator we can a dc for the circuit. For the regulation, zener diode is not preferred because of its parasitic capacitance. Some CMOS circuits based on voltage reference may be used.

III. PSEUDO-RESISTORS

The Pseudo-resistors plays a vital role in the realization of low frequency high pass function, in order to avoid large on-chip capacitor resulting high power consumption and poor SNR. The resistors of the order of several Giga- ohms are needed for this circuit. There are six different structures as shown in the figure3. The linear variation of current for each structure is plotted for comparison. The fig 3. (a,b) shows the uni-linear, resulting noise disturbance is more.

The transfer characteristics for single and anti-parallel connected is shown in the figure4. From this I-V curve we can understand the anti-parallel connected (DoubDio & DoubSG) pseudo resistor exhibits bilinear characteristics. The figure3.(e,f) uses sub-threshold PMOS and deep-depletion NMOS respectively. In both cases, it needs additional biasing for tuning purpose. For implantable applications, the supply is applied externally through inductive coupling. Therefore the design with large number of biasing is not preferred. Figure3. (c,d) shows bilinear characteristics and doesn’t require additional biasing for tuning purpose. Out of these two, Figure3.c is better suited for this application due to high linearity. The linear resistance curve is shown in figure5.
The drain current of PMOS transistor operating in sub-threshold region is

\[ I_d = I_o \left[ 1 - \exp \left( \frac{V_d}{V_t} \right) \right] \exp \left( \frac{V_g - V_{th} - V_{eff}}{nV_t} \right) \]

(1)

Where, \( I_d \) = drain Current; \( V_d \) = source-drain voltage; \( V_t \) = thermal voltage; \( V_{th} \) = threshold voltage; \( n \) = sub-threshold swing parameter; \( V_g \) = gate-source voltage.

The differential resistance \( \partial R \) can be obtained by differentiating \( I_d \) with respect to \( V_d \).

\[ \frac{\partial I_d}{\partial V_d} = \frac{1}{R_{out}} = \frac{I_o}{V_t} \cdot \exp \left( \frac{V_g - V_{th} - V_{eff}}{nV_t} \right) \cdot \exp \left( \frac{V_d}{V_t} \right) \]

(2)

The output of LNA. Second, it removes the EMG noise spectrum which resides within 100Hz. This circuit is built by the pseudo-resistors, in order to avoid the high power consumption. The mid-band gain value is set by the capacitors C1 and C2[8]. For bio-medical implantable applications, mid band – gain normally chosen by the ratio of c1 and c2 as 50. We can use either open loop or closed loop configuration as shown in figure 6.

Simulation results show that the open loop configuration is better due to the high gain and low power consumption. No stability problem arises around the region of interest.

Figure 6(a). Gain Comparison between open loop and closed loop configuration

V. LOW NOISE AMPLIFIER (LNA)

This circuit serves two purposes. First, it avoids the DC voltage value of the body fluid where the MEAs are placed, because DC voltage may saturate...
A Fully Integrated Neural Signal Acquisition Amplifier for Epileptic Seizure Prediction

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VI. LNA NOISE ANALYSIS

Channel thermal noise of a MOSFET is derived from the noise current equation.
\[
i_{n}^{2} = 4kBTg_m
\]
(3)
Where, \( k \) – Boltzmann Constant; \( T \) – Absolute Temperature; \( g_m \) = transconductance.
The factor is a complex function of the basic transistor parameters and bias conditions. For modern CMOS processes with oxide thickness in the order of 50nm and with a lower substrate doping \( N_b \) of about \( 10^{15} \) – \( 10^{16} \) cm\(^{-3}\), the factor is between 0.67 and 1[9].

\[
\nu_{n,input}^{2} = \frac{8kBT}{g_{m1}} \left[ 1 + \frac{g_m}{g_{n1}} \frac{g_{n2}}{g_{m1}} + \frac{g_{n3}}{g_{m1}} \right]^{2}
\]
(4)
Therefore, to reduce input-referred thermal noise, the W/L ratios of M1&M2 and the lengths of M1 & M2 are chosen to be very large, thereby maximizing the transconductance of M1 & M2, while minimizing those of M9 and M10. The input devices are the primary source of flicker noise; therefore large area PMOS transistors are used.

VII. LOW PASS FILTER

High linear, OTA-C filter based simple Low pass filter is shown in the figure10. Linearity of the low pass filter is improved by source degeneration topology. In this circuit the transistors biased on triode region. M25-M26 work in a saturation-active mode for positive \( V_{in} \) in an active-saturation mode for negative \( V_{in} \). Can result in a linear operation. The linear range is limited to \( V_{in} < V_{DSS} \).

The transconductance value for this low pass filter can be calculated from the equation given below.

\[
g_m \approx \frac{g_{m17}}{1 + \frac{g_{m2}}{4g_{m2}}}
\]
(5)

VIII. THE BULK DRIVEN SIGNAL PROCESSOR

For implantable bio-medical applications, gate-driven MOSFET posing threshold voltage constraint. A new processor using bulk-driven MOSFET has been developed to handle very small signals in the range of several millivolts. Both, bulk-driven and gate-driven performances are same except the physical size of former is small. The first order
equation shows the $V_{BS}$ and its effect on drain current.

$$i_D = K \left( V_{GS} - V_T - \frac{2}{3} V_{DS} \right) V_{DS} \quad \rightarrow \quad V_{DS} \geq V_{DS,MIN}$$

$$i_D = K \left( V_{GS} - V_T \right)^2 \left( 1 + \lambda V_{GS} \right) \quad \rightarrow \quad V_{GS} \geq V_{GS,MIN}$$

Where, $\lambda = 1 - \frac{2}{3} \frac{1}{2^{(1 - \sqrt{1 + \frac{1}{2} \frac{V_{GS}}{V_T}})}}$; $V_{GS,MIN} = \frac{V_{GS} - V_T}{\lambda}$

$$V_T = V_{TH} + \sqrt{2 \phi V - V_{GS1} + \frac{1}{2} \phi}$$

The seizure onset from the neural signal can be clipped-off by the processor. Later, it compared with the reference signal using high speed latch comparator. Thereby, seizure onset can be detected.

The circuit used to extract the seizure onset is shown in the figure 11. Neural signal from the amplifier is applied at the bulk of transistor $M_A$. Here, gate and source is tied to make $V_{GS}$ constant. Therefore, the output variation is only due to bulk potential. When input is greater than zero, reverse depletion layer is formed and it causes current to flow through the transistor $M_A$. The neural reference potential $V_{SYN}$ for the normal behavior is applied to the bulk of $M_B$.

The combination of $M_A$ & $M_B$ blocks all signal whose value is less than the reference potential($V_{SYN}$). Therefore the onset feature can be extracted.

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<th>TABLE 1: DEVICE SIZING</th>
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<td><strong>Device Sizing</strong></td>
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<td><strong>Devices</strong></td>
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IX. CONCLUSION

The neural signal acquisition amplifier with 18.24μW and 1.24μVrms over the 100Hz – 5 KHz has been presented. A new signal processing circuit has been developed using 2 transistor reduces overall power consumption. Simulation results shows that this circuit is designed to meet all requirements for the detection and forewarning to the epilepsy affected patients for safety and clinical contexts.

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REFERENCES