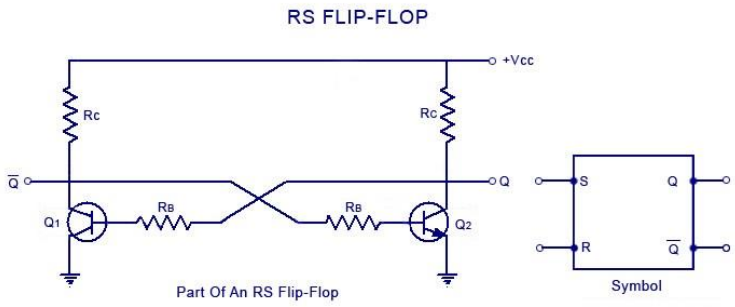
555 TIMER BASICS

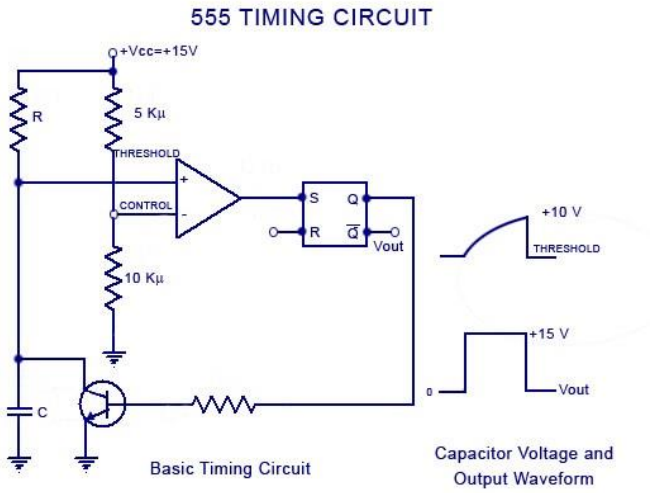
The **555 timer** combines a relaxation oscillator, two comparators, an R-S flip-flop, and a discharge capacitor.



R-S Flip-Flop: – A pair of cross-coupled transistors is shown in figure. Each collector drives the opposite base through resistance R_B. In such circuit one transistor is saturated while the other is cut-off. For instance, if transistor Q_1 is saturated, its collector voltage is almost zero. So there is no base drive for transistor Q_2 and it goes into cut-off and its collector voltage approaches + V_{CC}. This high voltage produces enough base current to keep transistor Q_1 in saturation.

On the other hand if transistor Q_1 is cut-off, its collector voltage, which is approximately equal to + V_{CC}, drives the transistor Q_2 into saturation. The low collector voltage (which is approximately to zero) of this transistor then keeps the transistor Q_2 in cut-off.Depending on which transistor is saturated, the Q output is either low or high. By adding more components to the circuit, an R-S flip-flop is obtained. R-S flip-flop is a circuit that can set the Q output to high or reset it low.Incidentally, a complementary (opposite) output Q is available from the collector of the other transistor.

Figure shows the schematic symbol for an R-S flip-flop of any design. The circuit latches in either two states. A high S input sets Q to high; a high R input resets Q to low. Output Q remains in a given state until it is triggered into the opposite state.



Basic Timing Concept

Figure illustrates some basic ideas that will prove useful in coming blog posts of the 555 timer. Assuming output Q high, the transistor is saturated and the capacitor voltage is clamped at ground i.e. the capacitor C is shorted and cannot charge.

The non-inverting input voltage of the comparator is referred to as the *threshold voltage* while the inverting input voltage is referred to as the *control voltage.* With R-S flip flop set, the saturated transistor holds the threshold voltage at zero. The control voltage, however, is fixed at 2/3 V_{CC} (i.e. at 10 V) because of the voltage divider.

Suppose that a high voltage is applied to the R input. This resets the flip-flop R-Output Q goes low and the transistor is cut-off. Capacitor C is now free to charge. As this capacitor C charges, the threshold voltage rises. Eventually, the threshold voltage becomes slightly greater than (+ 10 V). The output of the comparator then goes high, forcing the R S flip-flop to set. The high Q output saturates the transistor, and this quickly discharges the capacitor. The two waveforms are depicted in figure. An exponential rise is across the capacitor C, and a positive going pulse appears at the output Q. Thus capacitor voltage V_C is exponential while the output is rectangular, as illustrated in figure.

Source : http://todayscircuits.blogspot.com/2011/06/555-timer-complete-basic-guide.html#.VUBpt9Kqqko