3-D CHIP DESIGN STRATEGY

It is clear from previous discussions that with the ever increasing chip complexity and functionalities interconnect delay problems are going to be worse in very deep submicron technology. 3-D IC (or interconnect) technologies such as ***wire-bonding***, ***micro-bumps***,***through-vias***, and ***contact less interconnect*** are promising solution for interconnect delay concerns. This technique helps in effective large scale integration of different systems on a single IC.

3-D IC design architecture consists of a number of blocks which are divided from a 2-D chip(s). Different silicon layers are stacked one above the other and different blocks are placed on different layers, known as "tier". Multiple layer of interconnects can be constructed in each Si tier. These interconnects are linked by ***vertical interconnects***. By routing vertical interconnects appropriately long wire length can be shortened. Multiple active routing layers enhances the options to place the critical path components close to each other thereby decreasing RC delay and significantly improve performance of the design. Global interconnects are made common to all layers. Long wire inter-block communication delay is eliminated by placing these blocks in different layers and connecting them by a vertical interconnect. Thus system design becomes flexible with 3-D IC architecture. Three-dimensional integration can reduce the wiring and hence reduce the capacitance, power dissipation, and chip area and therefore improve overall performance of the chip.

The powerful advantage of 3-D chip design methodology can be exploited to build System on Chips (SoCs). Circuits with different voltage and performance requirements such as digital and analog components in the mixed-signal systems can be placed in different layers as shown in the Figure (1).

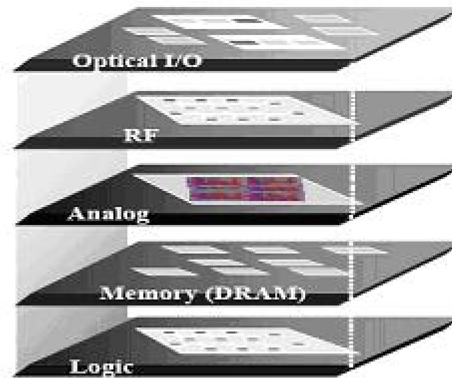

Figure (1) Block representation of 3-D IC [5]

Blocks are placed in different layers have lesser electromagnetic interference noise. This can achieve better noise performance of the intended design. High performance SoCs requires synchronous clock distribution. At the topmost layer of the 3-D IC ***optical interconnects*** and I/Os can be employed to achieve this.

Source : http://asic-soc.blogspot.in/2007/10/3-d-chip-design-strategy.html