

# 3D PACKAGING; DECISION TIME FOR 3D TEST

The decision to use stacked die or TSV-enabled devices is intertwined with cost considerations – there are no surprises on that point. However, Risto Puhakka, president, VLSI Research, emphasizes that the decision to go to 3D packaging is a technology play, not a cost play. No matter how demanding companies are in their insistence on lowering the cost of 3D packaging, it will still cost more than today's packaging solutions. "The challenge is how to get more money out of the device/package," said Puhakka.

VLSI Research believes that implementation of 3D packaging will happen in the areas where there's enough bang for the buck. "It probably lends itself to very high-end server applications, and maybe some high-end mobile," said Puhakka. "But mainstream PC or mainstream tablet – no way!" Well, at least not for a while. Because of the cost sensitivity of the memory segment, Puhakka thinks the industry will likely see only some 3D memory applications in either late 2012, or in 2013, and in very narrow segments at that. "The DRAM production year is 2012, but there will only be a 10% market penetration by 2016," said Puhakka (Fig. 1).

“For processors, we expect production in 2014 and by 2016, 25% will be using it.”

Testing 3D devices is often considered to be a very big challenge, but Puhakka sees no roadblocks there. “We don’t see any problem on the horizon, and the EDA companies are addressing the issues.”

E. Jan Vardaman, president and founder of TechSearch International, observes that while the drivers for 3D TSV remain constant, the timeline for its adoption keeps shifting out. A key to this technology entering high-volume manufacturing (HVM) is resolving the technical and business issues. “One of the main technical issues is in the wafer thinning process, specifically the debond step,” noted Vardaman.

“Several companies are developing new materials that may improve yield and new equipment may also be introduced in the future.”

Vardaman also pointed out that the “known good die” methodology is a requirement to provide high enough yield to make TSV processes cost-effective.

“Companies are still discussing issues such as whether to probe or not to probe wafers, the use of built-in self-test (BIST), and required test methodologies,” said Vardaman. “Until all issues are resolved with 3D TSV, alternatives including stacked die, chip-on-chip (CoC), and package-on-package (PoP) will flourish.”

TechSearch International’s data indicates that 600 million PoPs shipped in 2011, and the number is expected to increase over the next few years. “Recent extensions to PoP, including ultra-thin embedded die PoP that can deliver a total package

thickness below 1mm will extend the life of PoP.” Steve Pateras, product marketing director for design-for-test (DfT) at Mentor Graphics, explained that the ability to enable comprehensive testing of all popular DRAMs and related TSV-based buses, and being able to generate high-quality tests for logic-on-logic stacks, were key challenges. The company’s Tessent platform addresses these issues by using a combination of hierarchical test architecture, high-compression scan testing, and BIST technologies. Making the case for BIST, Pateras observed that there is a dual value in adopting it for 3D ICs. “You get more efficient wafer sort testing, and those same resources can be used for retesting within the stack,” said Pateras.

Wafer sort testing also has to be much better when going to 3D-ICs. Testing of high-speed I/O, for example, is particularly challenging if done by making physical contact (resulting in physical damage upon touchdown, or physical space limitations). Fixturing at the wafer-scale level can also have performance issues related to reflection and inductance, making it difficult to get high-speed accuracy. To address these problems, Mentor uses contact-less solutions whereby delay-based measurements can be done.

Source: <http://electroi.com/mysemicondaily/2012/07/11/a-technology-play-for-3d-packaging-decision-time-for-3d-test/>