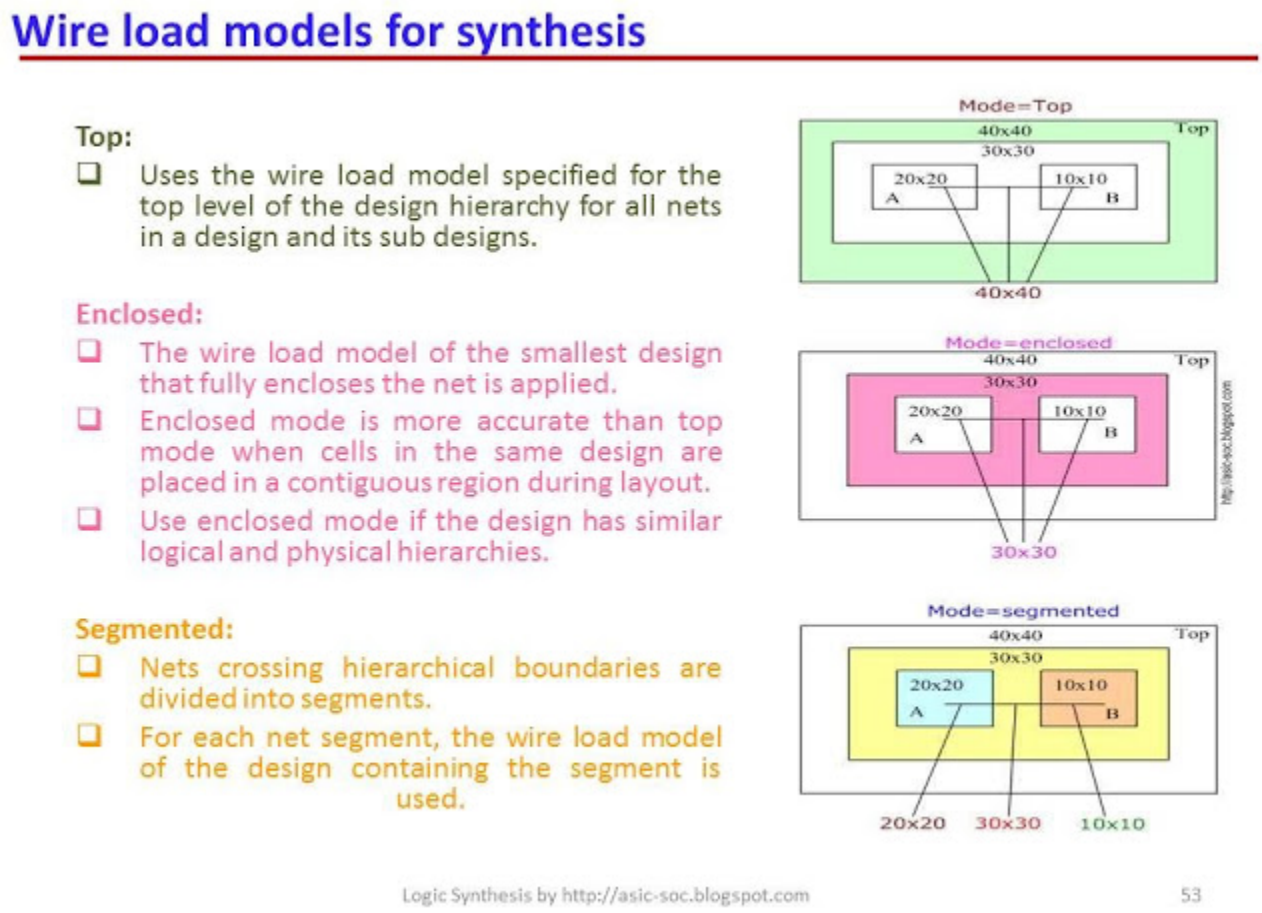
WIRE LOAD MODELS FOR SYNTHESIS

Wire load modeling allows us to estimate the effect of wire length and fanout on the resistance, capacitance, and area of nets. Synthesizer uses these physical values to calculate wire delays and circuit speeds. Semiconductor vendors develop wire load models, based on statistical information specific to the vendors' process. The models include coefficients for area, capacitance, and resistance per unit length, and a fanout-to-length table for estimating net lengths (the number of fanouts determines a nominal length).



Selection of wire load models in the initial stage (before physical design) depends on the fallowing factors:

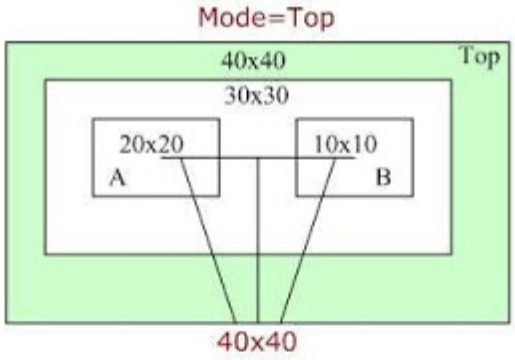
1. User specification
2. Automatic selection based on design area
3. Default specification in the technology library

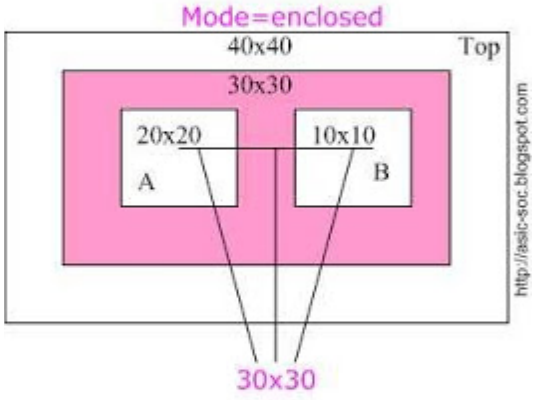
Once the final routing step is over in the physical design stage, wire load models are generated based on the actual routing in the design and synthesis is redone using those wire load models.

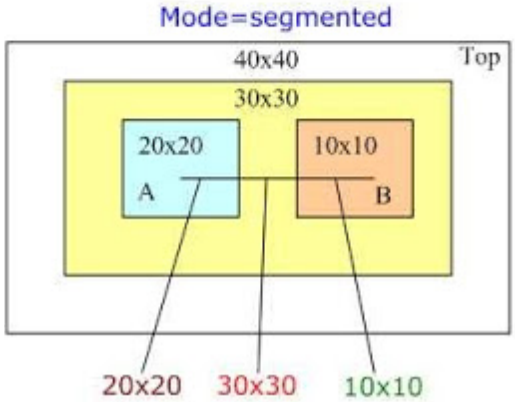
In hierarchical designs, we have to determine which wire load model to use for nets that cross hierarchical boundaries. There are three modes for determining which wire load model to use for nets that cross hierarchical boundaries:

9.1.1 Top:

Applying same wire load models to all nets as if the design has no hierarchy and uses the wire load model specified for the top level of the design hierarchy for all nets in a design and its sub designs.







9.1.2 Enclosed:

The wire load model of the smallest design that fully encloses the net is applied. If the design enclosing the net has no wire load model, then traverses the design hierarchy upward until we finds a wire load model. Enclosed mode is more accurate than top mode when cells in the same design are placed in a contiguous region during layout.

Use enclosed mode if the design has similar logical and physical hierarchies.

9.1.3 Segmented:

Wire load model for each segment of a net is determined by the design encompassing the segment. Nets crossing hierarchical boundaries are divided into segments. For each net segment, the wire load model of the design containing the segment is used. If the design contains a segment that has no wire load model, then traverse the design hierarchy upward until it finds a wire load model.

Source : http://asic-soc.blogspot.in/2013/07/wire-load-models-for-synthesis.html