Module 1

Power Semiconductor Devices

Lesson 4

Thyristors and Triacs

Instructional objects

On completion the student will be able to

- Explain the operating principle of a thyristor in terms of the “two transistor analogy”.
- Draw and explain the i-v characteristics of a thyristor.
- Draw and explain the gate characteristics of a thyristor.
- Interpret data sheet rating of a thyristor.
- Draw and explain the switching characteristics of a thyristor.
- Explain the operating principle of a Triac.

4.1 Introduction

Although the large semiconductor diode was a predecessor to thyristors, the modern power electronics area truly began with advent of thyristors. One of the first developments was the publication of the P-N-P-N transistor switch concept in 1956 by J.L. Moll and others at Bell Laboratories, probably for use in Bell's Signal application. However, engineers at General Electric quickly recognized its significance to power conversion and control and within nine months announced the first commercial Silicon Controlled Rectifier in 1957. This had a continuous current carrying capacity of 25A and a blocking voltage of 300V. Thyristors (also known as the Silicon Controlled Rectifiers or SCRs) have come a long way from this modest beginning and now high power light triggered thyristors with blocking voltage in excess of 6kv and continuous current rating in excess of 4kA are available. They have reigned supreme for two entire decades in the history of power electronics. Along the way a large number of other devices with broad similarity with the basic thyristor (invented originally as a phase control type device) have been developed. They include, inverter grade fast thyristor, Silicon Controlled Switch (SCS), light activated SCR (LASCR), Asymmetrical Thyristor (ASCR) Reverse Conducting Thyristor (RCT), Diac, Triac and the Gate turn off thyristor (GTO).

From the construction and operational point of view a thyristor is a four layer, three terminal, minority carrier semi-controlled device. It can be turned on by a current signal but can not be turned off without interrupting the main current. It can block voltage in both directions but can conduct current only in one direction. During conduction it offers very low forward voltage drop due to an internal latch-up mechanism. Thyristors have longer switching times (measured in tens of μs) compared to a BJT. This, coupled with the fact that a thyristor can not be turned off using a control input, have all but eliminated thyristors in high frequency switching applications involving a DC input (i.e, choppers, inverters). However in power frequency ac applications where the current naturally goes through zero, thyristor remain popular due to its low conduction loss its reverse voltage blocking capability and very low control power requirement. In fact, in very high power (in excess of 50 MW) AC – DC (phase controlled converters) or AC – AC (cyclo-converters) converters, thyristors still remain the device of choice.

4.2 Constructional Features of a Thyristor

Fig 4.1 shows the circuit symbol, schematic construction and the photograph of a typical thyristor.

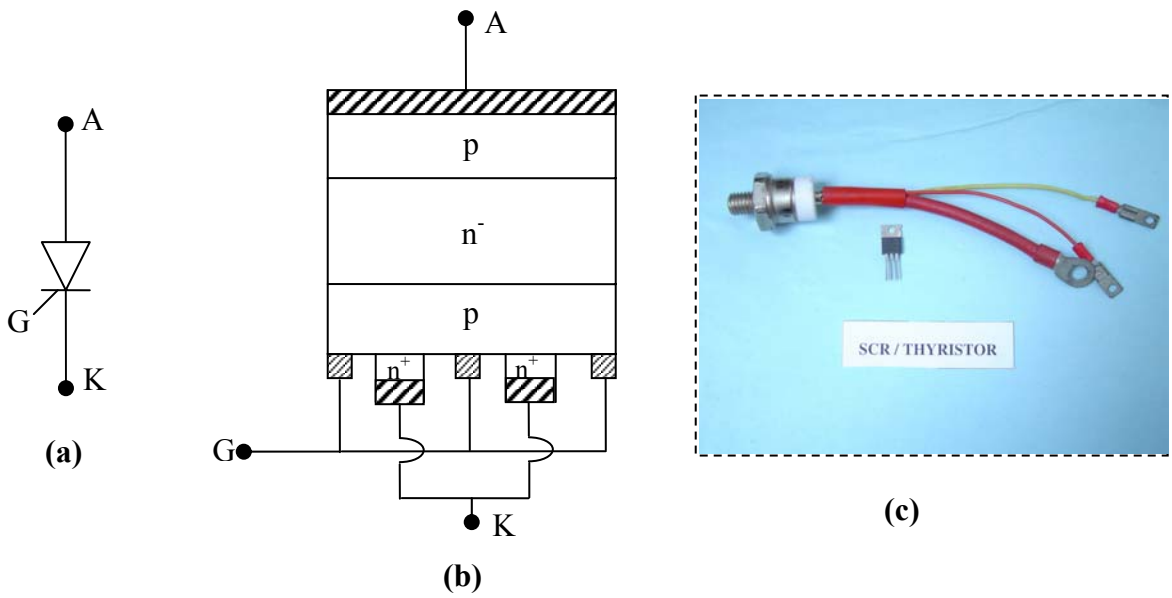


Fig. 4.1: Constructional features of a thysistor
(a) Circuit Symbol, (b) Schematic Construction, (c) Photograph

As shown in Fig 4.1 (b) the primary crystal is of lightly doped $\mathbf{n^-}$ type on either side of which two **p** type layers with doping levels higher by two orders of magnitude are grown. As in the case of power diodes and transistors depletion layer spreads mainly into the lightly doped $\mathbf{n^-}$ region. The thickness of this layer is therefore determined by the required blocking voltage of the device. However, due to conductivity modulation by carriers from the heavily doped p regions on both side during ON condition the "ON state" voltage drop is less. The outer n^+ layers are formed with doping levels higher then both the p type layers. The top **p** layer acls as the "Anode" terminal while the bottom $\mathbf{n^+}$ layers acts as the "Cathode". The "Gate" terminal connections are made to the bottom **p** layer.

As it will be shown later, that for better switching performance it is required to maximize the peripheral contact area of the gate and the cathode regions. Therefore, the cathode regions are finely distributed between gate contacts of the **p** type layer. An "Involute" structure for both the gate and the cathode regions is a preferred design structure.

4.3 Basic operating principle of a thyristor

The underlying operating principle of a thyristor is best understood in terms of the "two transistor analogy" as explained below.

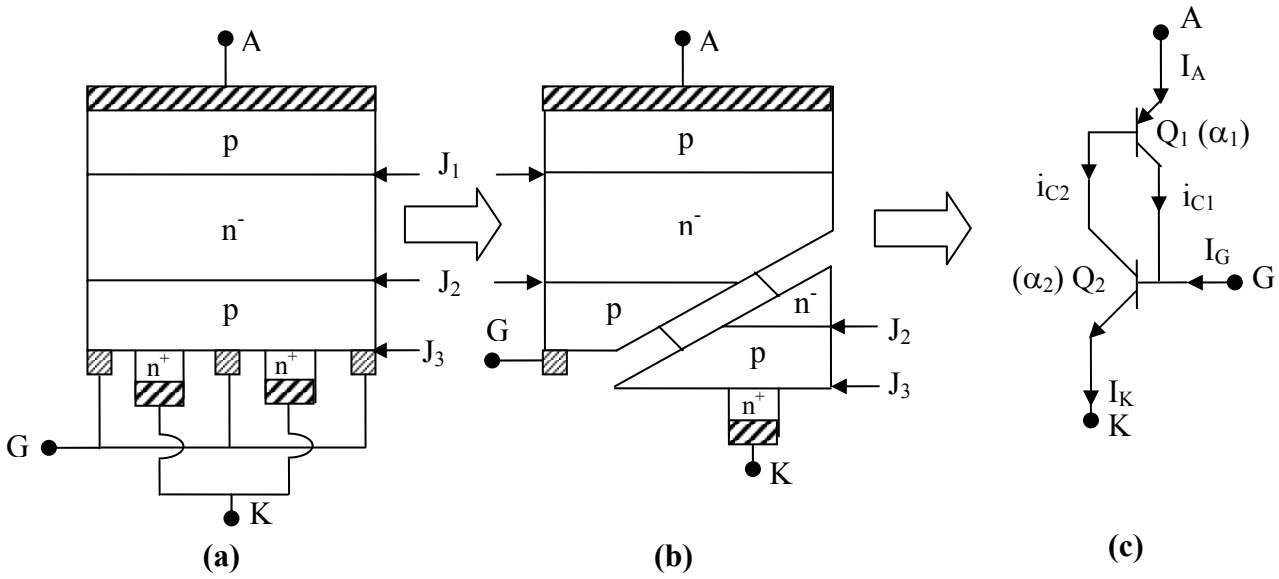


Fig. 4.2: Two transistor analogy of a thyristor construction.
(a) Schematic Construction, (b) Schematic division in component transistor
(c) Equivalent circuit in terms of two transistors.

a) Schematic construction,

b) Schematic division in component transistor

c) Equivalent circuit in terms of two transistors.

Let us consider the behavior of this p n p n device with forward voltage applied, i.e anode positive with respect to the cathode and the gate terminal open. With this voltage polarity J_1 & J_3 are forward biased while J_2 reverse biased.

Under this condition.

$$ic_1 = \alpha_1 I_A + I_{co1} \quad (4.1)$$

$$ic_2 = \alpha_2 I_K + I_{co2} \quad (4.2)$$

Where α_1 & α_2 are current gains of Q_1 & Q_2 respectively while I_{co1} & I_{co2} are reverse saturation currents of the CB junctions of Q_1 & Q_2 respectively.

Now from Fig 4.2 (c).

$$i_{c1} + i_{c2} = I_A \quad (4.3)$$

$$\& \; I_A = I_K \quad (4.4) \; (\because I_G = 0)$$

Combining Eq 4.1 & 4.4

$$I_A = \frac{I_{co1} + I_{co2}}{1 - (\alpha_1 + \alpha_2)} = \frac{I_{co}}{1 - (\alpha_1 + \alpha_2)} \quad (4.5)$$

Where $I_{co} \triangleq I_{co1} + I_{co2}$ is the total reverse leakage current of J_2

Now as long as V_{AK} is small I_{co} is very low and both $\propto_1$ & $\propto_2$ are much lower than unity. Therefore, total anode current I_A is only slightly greater than I_{co}. However, as V_{AK} is increased up to the avalanche break down voltage of J_2, I_{co} starts increasing rapidly due to avalanche multiplication process. As I_{co} increases both $\propto_1$ & $\propto_2$ increase and $\propto_1 + \propto_2$ approaches unity. Under this condition large anode current starts flowing, restricted only by the external load resistance. However, voltage drop in the external resistance causes a collapse of voltage across the thyristor. The CB junctions of both Q_1 & Q_2 become forward biased and the total voltage drop across the device settles down to approximately equivalent to a diode drop. The thyristor is said to be in "ON" state.

Just after turn ON if I_a is larger than a specified current called the Latching Current I_L, $\propto_1$ and $\propto_2$ remain high enough to keep the thyristor in ON state. The only way the thyristor can be turned OFF is by bringing I_A below a specified current called the holding current (I_H) where upon $\propto_1$ & $\propto_2$ starts reducing. The thyristor can regain forward blocking capacity once excess stored charge at J_2 is removed by application of a reverse voltage across A & K (ie, K positive with respect A).

It is possible to turn ON a thyristor by application of a positive gate current (flowing from gate to cathode) without increasing the forward voltage across the device up to the forward break-over level. With a positive gate current equation 4.4 can be written as

$$I_K = I_A + I_G \qquad (4.6)$$

Combining with Eqns. 4.1 to 4.3 $$I_A = \frac{\propto_2 I_G + I_{co}}{1 - (\propto_1 + \propto_2)} \qquad (4.7)$$

Obviously with sufficiently large I_G the thyristor can be turned on for any value of I_{co} (and hence V_{AK}). This is called gate assisted turn on of a Thyristor. This is the usual method by which a thyristor is turned ON.

When a reverse voltage is applied across a thyristor (i.e, cathode positive with respect to anose.) junctions J_1 and J_3 are reverse biased while J_2 is forward biased. Of these, the junction J_3 has a very low reverse break down voltage since both the $\mathbf{n}^+$ and **p** regions on either side of this junction are heavily doped. Therefore, the applied reverse voltage is almost entirely supported by junction J_1. The maximum value of the reverse voltage is restricted by

a) The maximum field strength at junction J_1 (avalanche break down)

b) Punch through of the lightly doped n^- layer.

Since the **p** layers on either side of the $\mathbf{n}^-$ region have almost equal doping levels the avalanche break down voltage of J_1 & J_2 are almost same. Therefore, the forward and the reverse break down voltage of a thyristor are almost equal.Up to the break down voltage of J_1 the reverse current of the thyristor remains practically constant and increases sharply after this voltage. Thus, the reverse characteristics of a thyristor is similar to that of a single diode.

If a positive gate current is applied during reverse bias condition, the junction J_3 becomes forward biased. In fact, the transistors Q_1 & Q_2 now work in the reverse direction with the roles of their respective emitters and collectors interchanged. However, the reverse $\propto_1$ & $\propto_2$ being significantly smaller than their forward counterparts latching of the thyristor does not occur. However, reverse leakage current of the thyristor increases considerably increasing the OFF state power loss of the device.

If a forward voltage is suddenly applied across a reverse biased thyristor, there will be considerable redistribution of charges across all three junctions. The resulting current can become large enough to satisfy the condition $\propto_1 + \propto_2 = 1$ and consequently turn on the thyristor. This is called dv/dt turn on of a thyristor and should be avoided.

Exercise 4.1

1) Fill in the blank(s) with the appropriate word(s)

i. A thyristor is a _____ carrier semi controlled device.

ii. A thyristor can conduct current in _____ direction and block voltage in _____ direction.

iii. A thyristor can be turned ON by applying a forward voltage greater than forward _____ voltage or by injecting a positive _____ current pulse under forward bias condition.

iv. To turn OFF a thyristor the anode current must be brought below _____ current and a reverse voltage must be applied for a time larger than _____ time of the device.

v. A thyristor may turn ON due to large forward _____.

Answers: (i) minority; (ii) one, both; (iii) break over, gate; (iv) holding, turn off; (v) dv/dt

2. Do you expect a thyristor to turn ON if a positive gate pulse is applied under reverse bias condition (i. e cathode positive with respect to anode)?

Answer: The two transistor analogy of thyristor shown in Fig 4.2 (c) indicates that when a reverse voltage is applied across the device the roles of the emitters and collectors of the constituent transistors will reverse. With a positive gate pulse applied it may appear that the device should turn ON as in the forward direction. However, the constituent transistors have very low current gain in the reverse direction. Therefore no reasonable value of the gate current will satisfy the turn ON condition (i.e.$\propto_1 + \propto_2 = 1$). Hence the device will not turn ON.

4.4 Steady State Characteristics of a Thyristor

4.4.1 Static output i-v characteristics of a thyristor

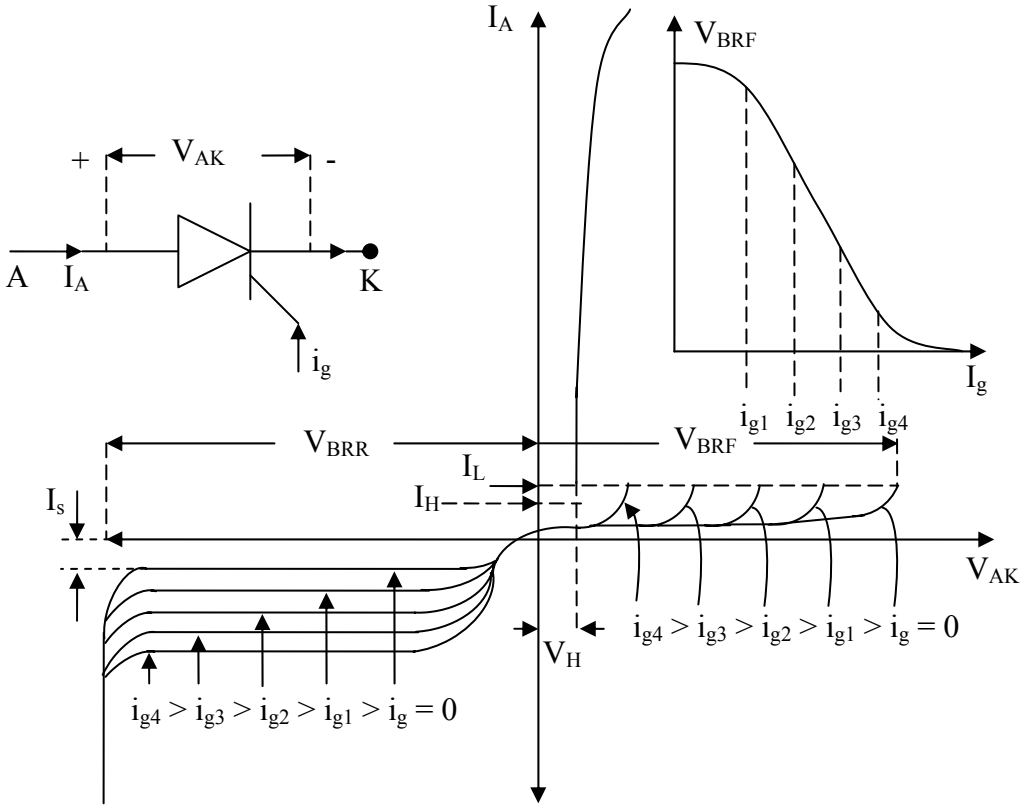


Fig. 4.3: Static output characteristics of a Thyristor

The circuit symbol in the left hand side inset defines the polarity conventions of the variables used in this figure.

With ig = 0, V_{AK} has to increase up to forward break over voltage V_{BRF} before significant anode current starts flowing. However, at V_{BRF} forward break over takes place and the voltage across the thyristor drops to V_H (holding voltage). Beyond this point voltage across the thyristor (V_{AK}) remains almost constant at V_H (1-1.5v) while the anode current is determined by the external load.

The magnitude of gate current has a very strong effect on the value of the break over voltage as shown in the figure. The right hand side figure in the inset shows a typical plot of the forward break over voltage (V_{BRF}) as a function of the gate current (I_g)

After "Turn ON" the thyristor is no more affected by the gate current. Hence, any current pulse (of required magnitude) which is longer than the minimum needed for "Turn ON" is sufficient to effect control. The minimum gate pulse width is decided by the external circuit and should be long enough to allow the anode current to rise above the latching current (I_L) level.

The left hand side of Fig 4.3 shows the reverse i-v characteristics of the thyristor. Once the thyristor is ON the only way to turn it OFF is by bringing the thyristor current below holding current (I_H). The gate terminal has no control over the turn OFF process. In ac circuits with resistive load this happens automatically during negative zero crossing of the supply voltage. This is called "natural commutation" or "line commutation". However, in dc circuits some arrangement has to be made to ensure this condition. This process is called "forced commutation."

During reverse blocking if $i_g = 0$ then only reverse saturation current (I_s) flows until the reverse voltage reaches reverse break down voltage (V_{BRR}). At this point current starts rising sharply. Large reverse voltage and current generates excessive heat and destroys the device. If $i_g > 0$ during reverse bias condition the reverse saturation current rises as explained in the previous section. This can be avoided by removing the gate current while the thyristor is reverse biased.

The static output i-v characteristics of a thyristor depends strongly on the junction temperature as shown in Fig 4.4.

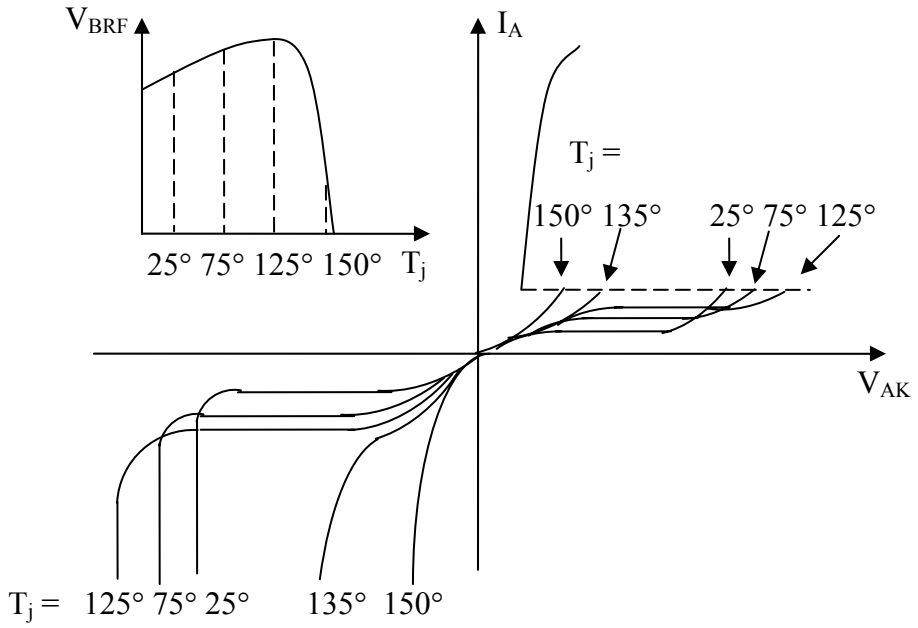


Fig. 4.4: Effect of junction temperature (T_j) on the output i – v characteristics of a thyristor.

4.4.2 Thyristor Gate Characteristics

The gate circuit of a thyristor behaves like a poor quality diode with high on state voltage drop and low reverse break down voltage. This characteristic usually is not unique even within the same family of devices and shows considerable variation from device to device. Therefore, manufacturer's data sheet provides the upper and lower limit of this characteristic as shown in Fig 4.5.

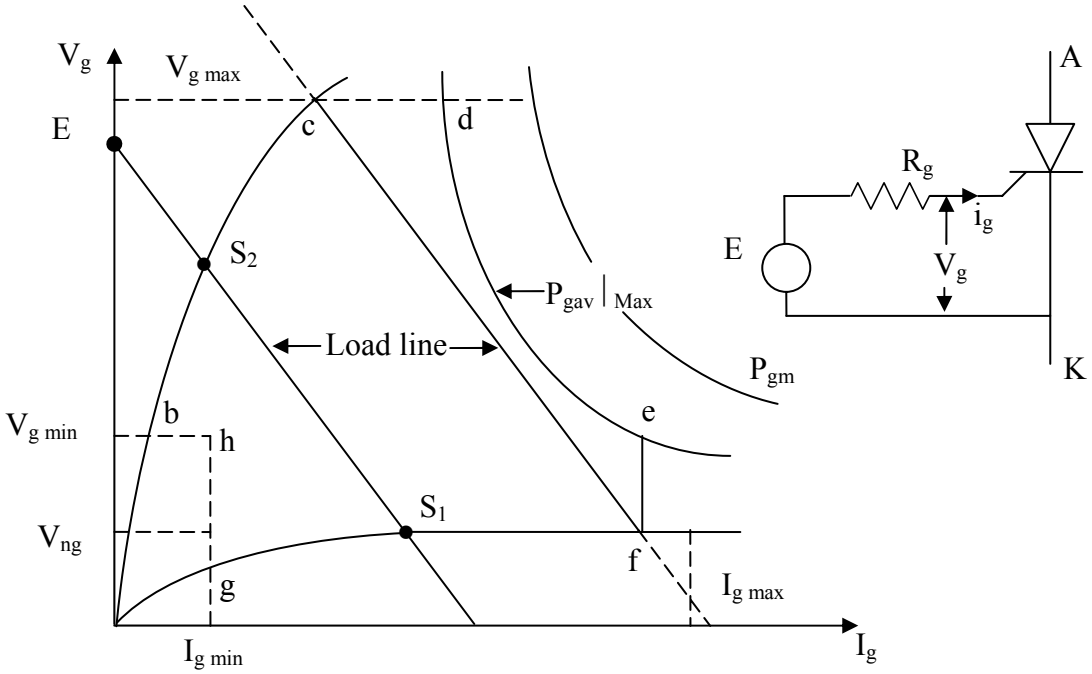


Fig. 4.5: Gate characteristics of a thyristor.

Each thyristor has maximum gate voltage limit (V_{gmax}), gate current limit (I_{gmax}) and maximum average gate power dissipation limit $\left(P_{gav}\big|_{Max}\right)$. These limits should not be exceeded in order to avoid permanent damage to the gate cathode junction. There are also minimum limits of V_g (V_{gmin}) and Ig (I_{gmin}) for reliable turn on of the thyristor. A gate non triggering voltage (V_{ng}) is also specified by the manufacturers of thyristors. All spurious noise signals should be less than this voltage V_{ng} in order to prevent unwanted turn on of the thyristor. The useful gate drive area of a thyristor is then b c d e f g h.

Referring to the gate drive circuit in the inset the equation of the load line is given by

$$V_g = E - R_g i_g$$

A typical load line is shown in Fig 4.5 by the line S_1 S_2.

The actual operating point will be some where between S_1 & S_2 depending on the particular device.

For optimum utilization of the gate ratings the load line should be shifted forwards the $P_{gav}\big|_{Max}$ curve without violating $V_g\big|_{Max}$ or I_{gMax} ratings. Therefore, for a dc source E **c f** represents the optimum load line from which optimum values of E & R_g can be determined.

It is however customary to trigger a thyristor using pulsed voltage & current. Maximum power dissipation curves for pulsed operation (P_{gm}) allows higher gate current to flow which in turn reduces the turn on time of the thyristor. The value of P_{gm} depends on the pulse width (T_{ON}) of the gate current pulse. T_{ON} should be larger than the turn on time of the thyristor. For T_{ON} larger

than 100 μs, average power dissipation curve should be used. For T_{ON} less than 100 μs the following relationship should be maintained.

$$\delta P_{gm} \le P_{gav}\Big|_{Max} \qquad (4.9)$$

Where $\delta = T_{ON}\ f_p$, $f_p =$ pulse frequency.

The magnitude of the gate voltage and current required for triggering a thyristor is inversely proportional to the junction temperature.

The gate cathode junction also has a maximum reverse (i.e, gate negative with respect to the cathode) voltage specification. If there is a possibility of the reverse gate cathode voltage exceeding this limit a reverse voltage protection using diode as shown in Fig 4.6 should be used.

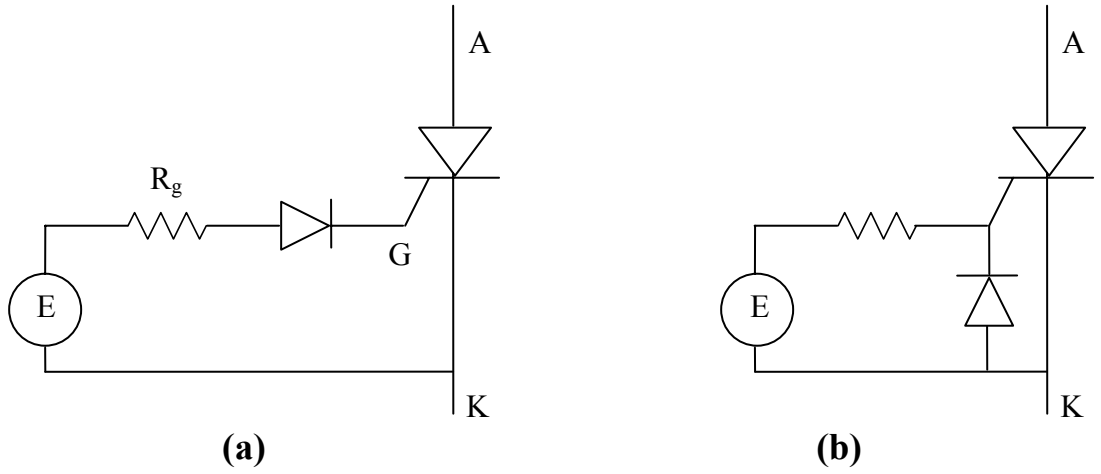


Fig. 4.6: Gate Cathode reverse voltage protection circuit.

Exercise 4.2

1) Fill in the blank(s) with the appropriate word(s)

i. Forward break over voltage of a thyristor decreases with increase in the _____ current.

ii. Reverse _____ voltage of a thyristor is _____ of the gate current.

iii. Reverse saturation current of a thyristor _____ with gate current.

iv. In the pulsed gate current triggering of a thyristor the gate current pulse width should be larger than the _____ time of the device.

v. To prevent unwanted turn ON of a thyristor all spurious noise signals between the gate and the cathode must be less than the gate _____ voltage.

Answer: (i) gate; (ii) break down, independent; (iii) increases; (iv) Turn ON; (v) non-trigger.

2) A thyristor has a maximum average gate power dissipation limit of 0.2 watts. It is triggered with pulsed gate current at a pulse frequency of 10 KHZ and duly ratio of 0.4. Assuming the gate cathode voltage drop to be 1 volt. Find out the allowable peak gate current magnitude.

Answer: On period of the gate current pulse is

$$T_{ON} = \delta T_S = \delta / fs = \frac{0.4}{10^4} \text{ sec} = 40\,\mu s < 100\,\mu s.$$

Therefore, pulsed gate power dissipation limit P_{gm} can be used. From Equation 4.9

$$\delta P_{gm} \leq P_{gav}(\text{Max})$$

$$\text{or } P_{gm} \leq \frac{0.2}{\delta} \text{ watts} = .5\text{watts}$$

But $P_{gm} = I_g V_g$; $V_g = 1V$ $\quad \therefore I_g\Big|_{Max} = \frac{.5}{1} = 0.5\text{Amps}.$

4.5 Thyristor ratings

Some useful specifications of a thyristor related to its steady state characteristics as found in a typical "manufacturer's data sheet" will be discussed in this section.

4.5.1 Voltage ratings

Peak Working Forward OFF state voltage (V_{DWM}): It specifics the maximum forward (i.e, anode positive with respect to the cathode) blocking state voltage that a thyristor can withstand during working. It is useful for calculating the maximum RMS voltage of the ac network in which the thyristor can be used. A margin for 10% increase in the ac network voltage should be considered during calculation.

Peak repetitive off state forward voltage (V_{DRM}): It refers to the peak forward transient voltage that a thyristor can block repeatedly in the OFF state. This rating is specified at a maximum allowable junction temperature with gate circuit open or with a specified biasing resistance between gate and cathode. This type of repetitive transient voltage may appear across a thyristor due to "commutation" of other thyristors or diodes in a converter circuit.

Peak non-repetitive off state forward voltage (V_{DSM}): It refers to the allowable peak value of the forward transient voltage that does not repeat. This type of over voltage may be caused due to switching operation (i.e, circuit breaker opening or closing or lightning surge) in a supply network. Its value is about 130% of V_{DRM}. However, V_{DSM} is less than the forward break over voltage V_{BRF}.

Peak working reverse voltage (V_{DWM}): It is the maximum reverse voltage (i.e, anode negative with respect to cathode) that a thyristor can with stand continuously. Normally, it is equal to the peak negative value of the ac supply voltage.

Peak repetitive reverse voltage (V_{RRM}): It specifies the peak reverse transient voltage that may occur repeatedly during reverse bias condition of the thyristor at the maximum junction temperature.

Peak non-repetitive reverse voltage (V_{RSM}): It represents the peak value of the reverse transient voltage that does not repeat. Its value is about 130% of V_{RRM}. However, V_{RSM} is less than reverse break down voltage V_{BRR}.

Fig 4.7 shows different thyristor voltage ratings on a comparative scale.

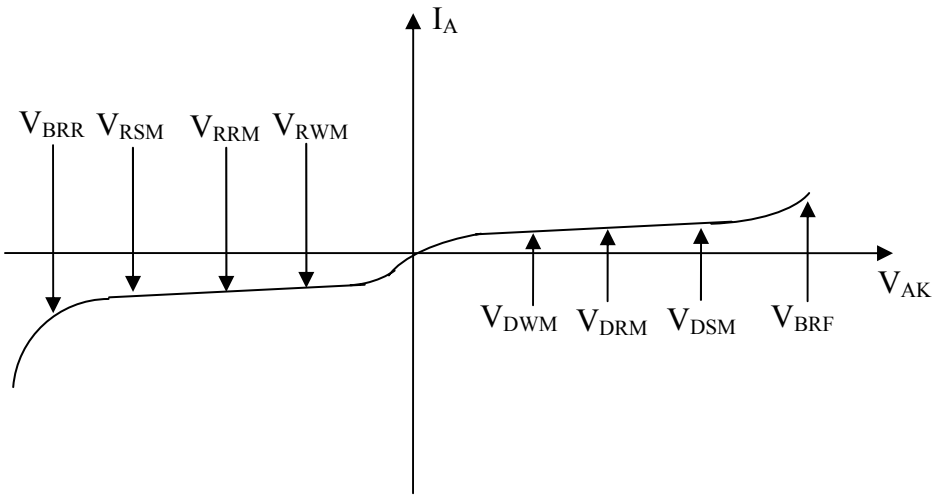


Fig. 4.7: Voltage ratings of a thyristor.

4.5.2 Current ratings

Maximum RMS current (I_{rms}): Heating of the resistive elements of a thyristor such as metallic joints, leads and interfaces depends on the forward RMS current I_{rms}. RMS current rating is used as an upper limit for dc as well as pulsed current waveforms. This limit should not be exceeded on a continuous basis.

Maximum average current (I_{av}): It is the maximum allowable average value of the forward current such that

i. Peak junction temperature is not exceeded

ii. RMS current limit is not exceeded

Manufacturers usually provide the "forward average current derating characteristics" which shows I_{av} as a function of the case temperature (T_c) with the current conduction angle ϕ as a parameter. The current wave form is assumed to be formed from a half cycle sine wave of power frequency as shown in Fig 4.8.

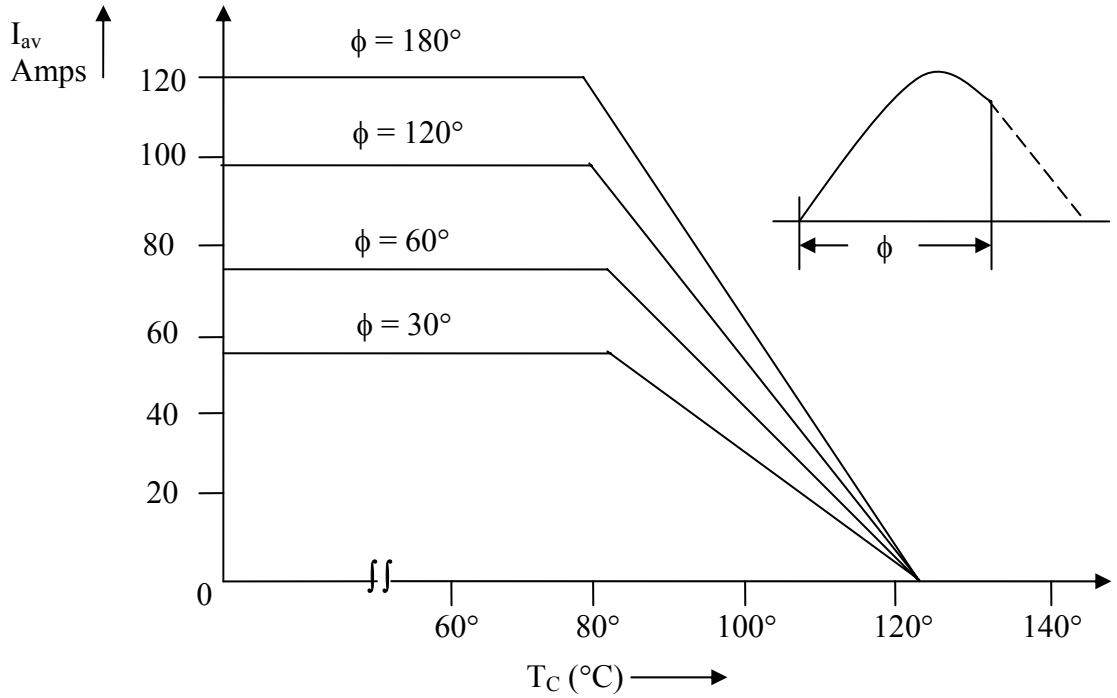


Fig. 4.8: Average forward current derating characteristics

Maximum Surge current (I_{SM}): It specifies the maximum allowable non repetitive current the device can withstand. The device is assumed to be operating under rated blocking voltage, forward current and junction temperation before the surge current occurs. Following the surge the device should be disconnected from the circuit and allowed to cool down. Surge currents are assumed to be sine waves of power frequency with a minimum duration of ½ cycles. Manufacturers provide at least three different surge current ratings for different durations.

For example

$I_{sM} = 3000$ A for $\frac{1}{2}$ cycle

$I_{sM} = 2100$ A for 3 cycles

$I_{sM} = 1800$ A for 5 cycles

Alternatively a plot of I_{sM} vs. applicable cycle numbers may also be provided.

Maximum Squared Current integral ($\int i^2 dt$): This rating in terms of A^2S is a measure of the energy the device can absorb for a short time (less than one half cycle of power frequency). This rating is used in the choice of the protective fuse connected in series with the device.

Latching Current (I_L): After Turn ON the gate pulse must be maintained until the anode current reaches this level. Otherwise, upon removal of gate pulse, the device will turn off.

Holding Current (I_H): The anode current must be reduced below this value to turn off the thyristor.

Maximum Forward voltage drop (V_F): Usually specified as a function of the instantaneous forward current at a given junction temperature.

Average power dissipation P_{av}): Specified as a function of the average forward current (I_{av}) for different conduction angles as shown in the figure 4.9. The current wave form is assumed to be half cycle sine wave (or square wave) for power frequency.

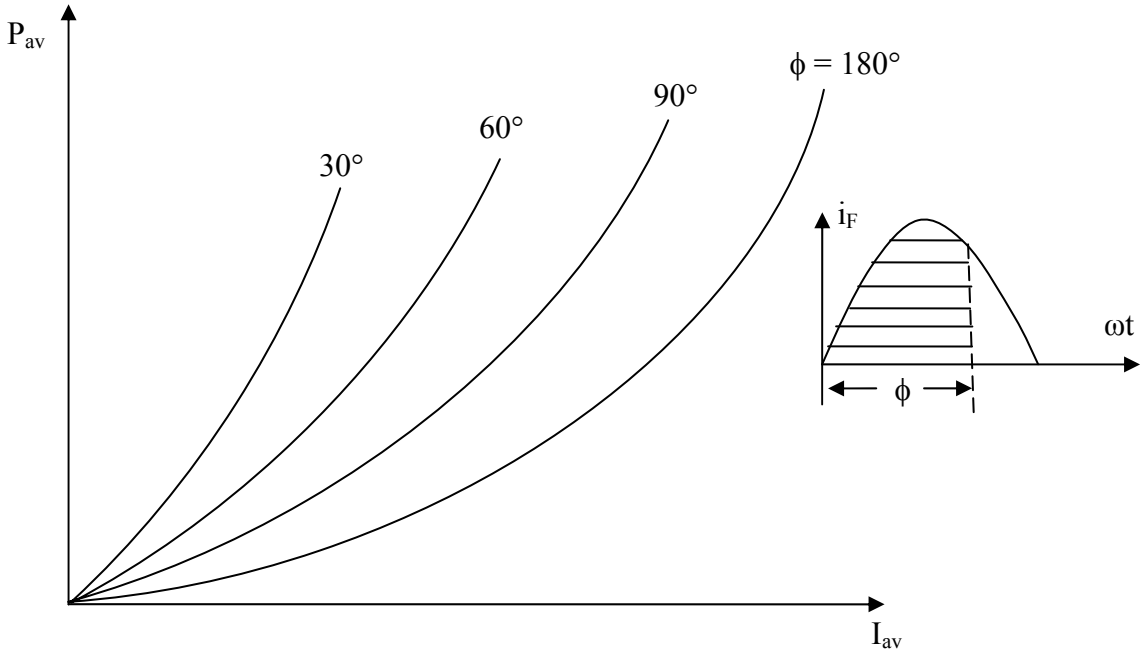


Fig. 4.9: Average power dissipation vs average forward current in a thyristor.

In the above diagram

$$I_{av} = \frac{1}{2\pi}\int_{o}^{\phi} i_F \, d\theta \qquad (4.10)$$

$$P_{av} = \frac{1}{2\pi}\int_{o}^{\phi} v_F \, i_F \, d\theta \qquad (4.11)$$

4.5.3 Gate Specifications

Gate current to trigger (I_{GT}): Minimum value of the gate current below which reliable turn on of the thyristor can not be guaranteed. Usually specified at a given forward break over voltage.

Gate voltage to trigger (V_{GT}): Minimum value of the gate cathode forward voltage below which reliable turn on of the thyristor can not be guaranteed. It is specified at the same break over voltage as I_{GT}.

Non triggering gate voltage (V_{GNT}): Maximum value of the gate-cathode voltage below which the thyristor can be guaranteed to remain OFF. All spurious noise voltage in the gate drive circuit must be below this level.

Peak reverse gate voltage (V_{GRM}): Maximum reverse voltage that can appear between the gate and the cathode terminals without damaging the junction.

Average Gate Power dissipation (P_{GAR}): Average power dissipated in the gate-cathode junction should not exceed this value for gate current pulses wider than 100 μs.

Peak forward gate current (I_{GRM}): The forward gate current should not exceed this limit even on instantaneous basis.

Exercise 4.3

1) Fill in the blank(s) with the appropriate word(s)

i. Peak non-repetitive over voltage may appear across a thyristor due to _____ or _____ surges in a supply network.

ii. V_{RSM} rating of a thyristor is greater than the _____ rating but less than the _____ rating.

iii. Maximum average current a thristor can carry depends on the _____ of the thyristor and the _____ of the current wave form.

iv. The I_{SM} rating of a thyristor applies to current waveforms of duration _____ than half cycle of the power frequency where as the $\int i^2dt$ rating applies to current durations _____ than half cycle of the power frequency.

v. The gate non-trigger voltage specification of a thyristor is useful for avoiding unwanted turn on of the thyristor due to _____ voltage signals at the gate.

Answer: (i) switching, lightning; (ii) V_{RRM}, V_{BRR}; (iii) case temperature, conduction angle; (iv) greater, less; (v) noise

2. A thyristor has a maximum average current rating 1200 Amps for a conduction angle of 180°. Find the corresponding rating for Φ = 60°. Assume the current waveforms to be half cycle sine wave.

Answer: The form factor of half cycle sine waves for a conduction angle ϕ is given by

$$F.F = \frac{I_{RMS}}{Iav} = \frac{\sqrt{\frac{1}{2\pi}\int_o^{\phi} Sin^2\theta \; d\theta}}{\frac{1}{2\pi}\int_o^{\phi} Sin\theta \; d\theta} = \frac{\sqrt{\pi\left(\phi - \frac{1}{2} Sin\, 2\phi\right)}}{1 - Cos\,\phi}$$

For $\phi = 180°$, $F.F = \frac{\pi}{2}$

$\therefore$ RMS current rating of the thyristor = $1200 \times \frac{\pi}{2} = 1885$ Amps.

For $\phi = 60°$, $F.F = 2\sqrt{\pi\left(\frac{\pi}{3} - \frac{\sqrt{3}}{4}\right)} = 2.778$

Since RMS current rating should not exceeded

Maximum I_{av} for $\phi = 60°$ $= \dfrac{1200 \times \pi}{4\sqrt{\pi\left(\pi/3 - \sqrt{3}/4\right)}} = 679.00$ Amps.

4.6 Switching Characteristics of a Thyristor

During Turn on and Turn off process a thyristor is subjected to different voltages across it and different currents through it. The time variations of the voltage across a thyristor and the current through it during Turn on and Turn off constitute the switching characteristics of a thyristor.

4.6.1 Turn on Switching Characteristics

A forward biased thyristor is turned on by applying a positive gate voltage between the gate and cathode as shown in Fig 4.10.

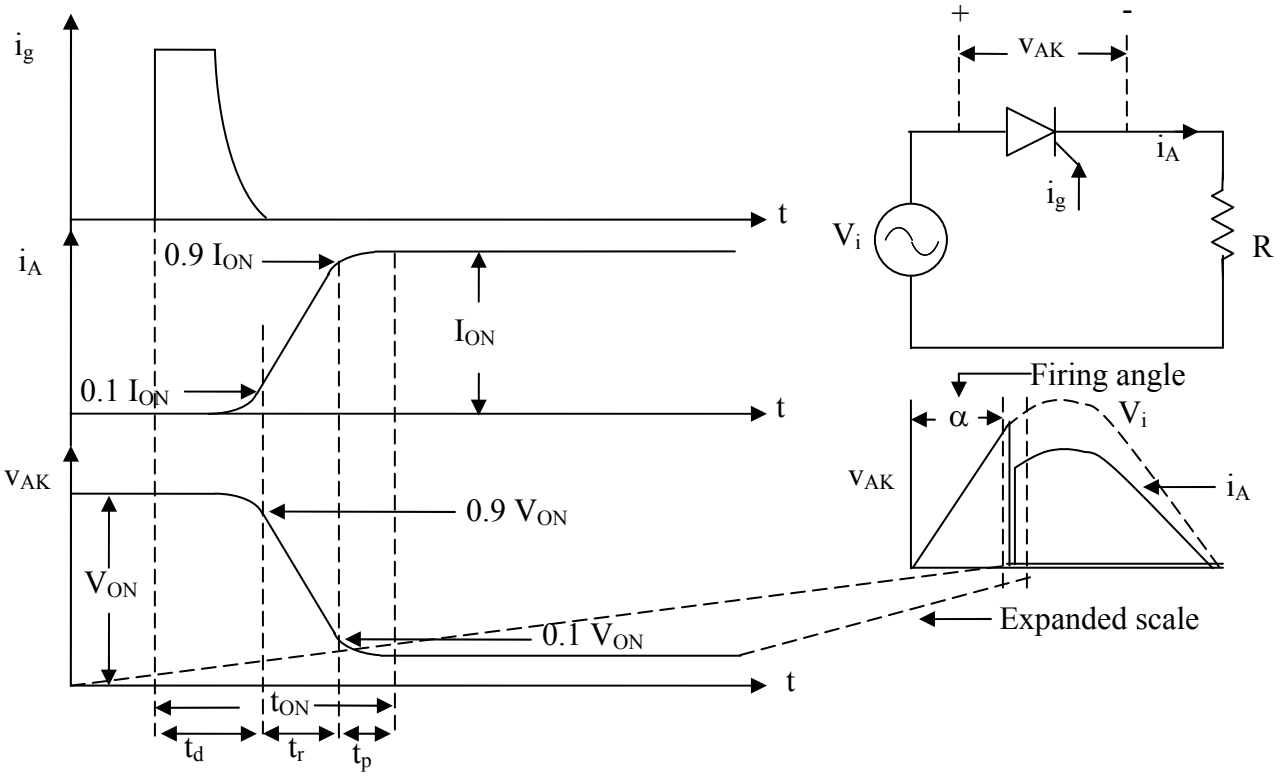


Fig. 4.10: Turn on characteristics of a thyristor.

Fig 4.10 shows the waveforms of the gate current (i_g), anode current (i_A) and anode cathode voltage (V_{AK}) in an expanded time scale during Turn on. The reference circuit and the associated waveforms are shown in the inset. The total switching period being much smaller compared to the cycle time, i_A and V_{AK} before and after switching will appear flat.

As shown in Fig 4.10 there is a transition time "t_{ON}" from forward off state to forward on state. This transition time is called the thyristor turn of time and can be divided into three separate intervals namely, (i) delay time (t_d) (ii) rise time (t_r) and (iii) spread time (t_p). These times are shown in Fig 4.10 for a resistive load.

Delay time (t_d): After switching on the gate current the thyristor will start to conduct over the portion of the cathode which is closest to the gate. This conducting area starts spreading at a finite speed until the entire cathode region becomes conductive. Time taken by this process constitute the turn on delay time of a thyristor. It is measured from the instant of application of the gate current to the instant when the anode current rises to 10% of its final value (or V_{AK} falls to 90% of its initial value). Typical value of "t_d" is a few micro seconds.

Rise time (tr): For a resistive load, "rise time" is the time taken by the anode current to rise from 10% of its final value to 90% of its final value. At the same time the voltage V_{AK} falls from 90% of its initial value to 10% of its initial value. However, current rise and voltage fall characteristics are strongly influenced by the type of the load. For inductive load the voltage falls faster than the current. While for a capacitive load V_{AK} falls rapidly in the beginning. However, as the current increases, rate of change of anode voltage substantially decreases.

If the anode current rises too fast it tends to remain confined in a small area. This can give rise to local "hot spots" and damage the device. Therefore, it is necessary to limit the rate of rise of the ON state current $\left(\frac{di_A}{dt}\right)$ by using an inductor in series with the device. Usual values of maximum allowable di_A/dt is in the range of 20-200 A/μs.

Spread time (tp): It is the time taken by the anode current to rise from 90% of its final value to 100%. During this time conduction spreads over the entire cross section of the cathode of the thyristor. The spreading interval depends on the area of the cathode and on the gate structure of the thyristor.

4.6.2 Turn off Switching Characteristics

Once the thyristor is on, and its anode current is above the latching current level the gate loses control. It can be turned off only by reducing the anode current below holding current. The turn off time t_q of a thyristor is defined as the time between the instant anode current becomes zero and the instant the thyristor regains forward blocking capability. If forward voltage is applied across the device during this period the thyristor turns on again.
During turn off time, excess minority carriers from all the four layers of the thyristor must be removed. Accordingly t_q is divided in to two intervals, the reverse recovery time (t_{rr}) and the gate recovery time (t_{qr}). Fig 4.11 shows the variation of anode current and anode cathode voltage with time during turn off operation on an expanded scale.

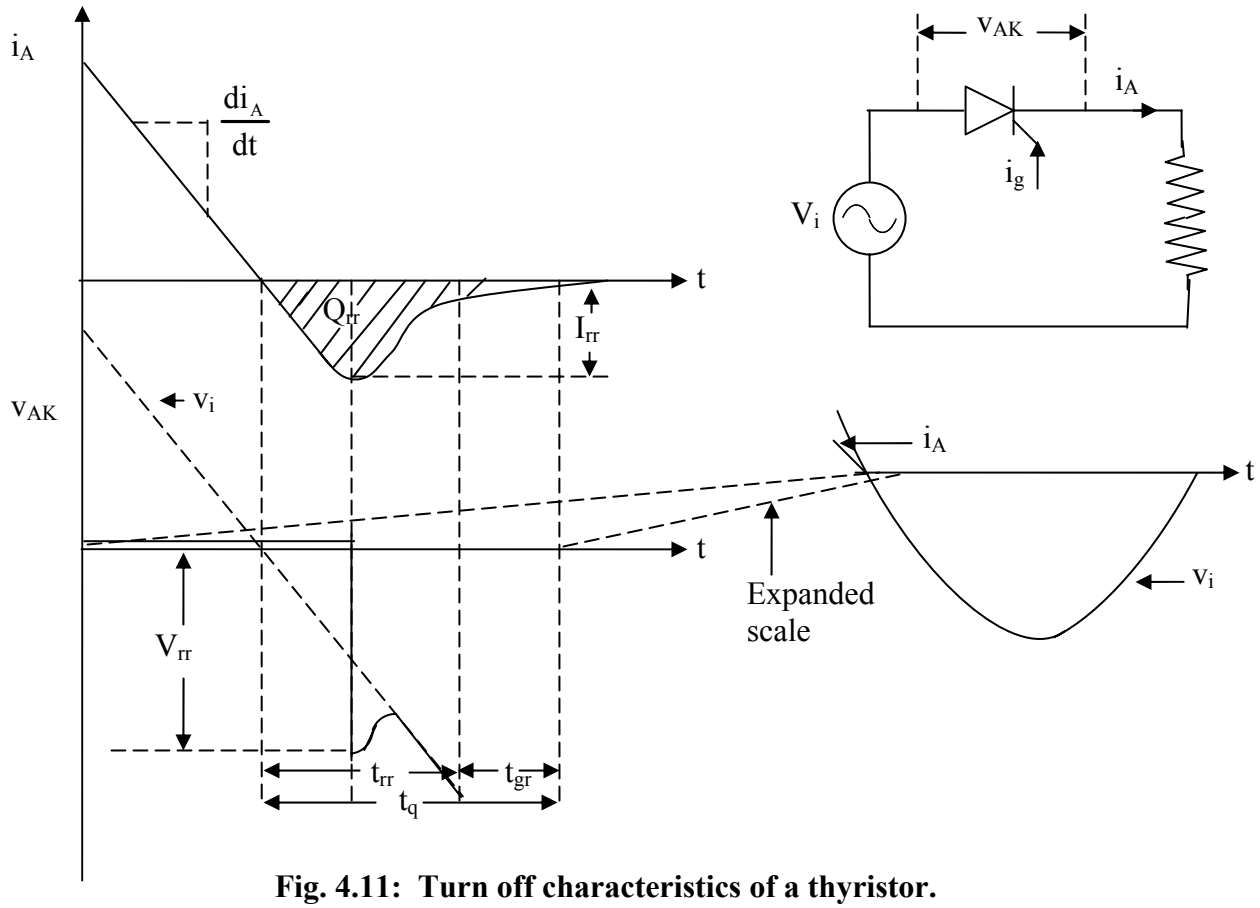


Fig. 4.11: Turn off characteristics of a thyristor.

The anode current becomes zero at time t_1 and starts growing in the negative direction with the same $\frac{di_A}{dt}$ till time t_2. This negative current removes excess carriers from junctions J_1 & J_3. At time t_2 excess carriers densities at these junctions are not sufficient to maintain the reverse current and the anode current starts decreasing. The value of the anode current at time t_2 is called the reverse recovery current (I_{rr}). The reverse anode current reduces to the level of reverse saturation current by t_3. Total charge removed from the junctions between t_1 & t_3 is called the reverse recovery charge (Q_{rr}). Fast decaying reverse current during the interval t_2 t_3 coupled with the $\frac{di}{dt}$ limiting inductor may cause a large reverse voltage spike (V_{rr}) to appear across the device. This voltage must be limited below the V_{RRM} rating of the device. Up to time t_2 the voltage across the device (V_{AK}) does not change substantially from its on state value. However, after the reverse recovery time, the thyristor regains reverse blocking capacity and V_{AK} starts following supply voltage v_i. At the end of the reverse recovery period (t_{rr}) trapped charges still exist at the junction J_2 which prevents the device from blocking forward voltage just after t_{rr}. These trapped charges are removed only by the process of recombination. The time taken for this recombination process to complete (between t_3 & t_4) is called the gate recovery time (t_{gr}). The time interval $t_q = t_{rr} + t_{gr}$ is called "device turn off time" of the thyristor.

No forward voltage should appear across the device before the time t_q to avoid its inadvertent turn on. A circuit designer must provide a time interval t_c ($t_c > t_q$) during which a reverse voltage is applied across the device. t_c is called the "circuit turn off time".

The reverse recovery charge Q_{rr} is a function of the peak forward current before turn off and its rate of decrease $\frac{di_A}{dt}$. Manufacturers usually provide plots of Q_{rr} as a function of di_A/dt for different values of peak forward current. They also provide the value of the reverse recovery current I_{rr} for a given I_A and di_A/dt. Alternatively I_{rr} can be evaluated from the given Q_{rr} characteristics following similar relationships as in the case of a **diode.**

As in the case of a diode the relative magnitudes of the time intervals t_1 t_2 and t_2 t_3 depends on the construction of the thyristor. In normal recovery "converter grade" thyristor they are almost equal for a specified forward current and reverse recovery current. However, in a fast recovery "inverter grade" thyristor the interval t_2 t_3 is negligible compared to the interval t_1 t_2. This helps reduce the total turn off time t_q of the thyristor (and hence allow them to operate at higher switching frequency). However, large voltage spike due to this "snappy recovery" will appear across the device after the device turns off. Typical turn off times of converter and inverter grade thyristors are in the range of 50-100 μs and 5-50 μs respectively.

As has been mentioned in the introduction thyristor is the device of choice at the very highest power levels. At these power levels (several hundreds of megawatts) reliability of the thyristor power converter is of prime importance. Therefore, suitable **protection arrangement** must be made against possible overvoltage, overcurrent and unintended turn on for each thyristor. At the highest power level (HVDC transmission system) thyristor converters operate from network voltage levels in excess of several hundreds of kilo volts and conduct several tens of kilo amps of current. They usually employ a large number of thyristors connected in **series parallel combination.** For maximum utilization of the device capacity it is important that each device in this series parallel combination share the blocking voltage and on state current equally. Special equalizing circuits are used for this purpose.

Exercise 4.4

1) Fill in the blank(s) with the appropriate word(s)

i. A thyristor is turned on by applying a _____ gate current pulse when it is _____ biased.

ii. Total turn on time of a thyristor can be divided into _____ time _____ time and _____ time.

iii. During rise time the rate of rise of anode current should be limited to avoid creating local _____.

iv. A thyristor can be turned off by bringing its anode current below _____ current and applying a reverse voltage across the device for duration larger than the _____ time of the device.

v. Reverse recovery charge of a thyristor depends on the _____ of the forward current just before turn off and its _____.

vi. Inverter grade thyristors have _____ turn off time compared to a converter grade thyristor.

Answer: (i) positive, forward; (ii) delay, rise, spread; (iii) hot spots (iv) holding, turn off; (v) magnitude, rate of decrease (vi) faster

2. With reference to Fig 4.10 find expressions for (i) turn on power loss and (ii) conduction power loss of the thyristor as a function of the firing angle $\propto$. Neglect turn on delay time and spread time and assume linear variation of voltage and current during turn on period. Also assume constant on state voltage V_H across the thyristor.

Answer: (i) For a firing angle $\propto$ the forward bias voltage across the thyristor just before turn on is

$$V_{ON} = \sqrt{2} V_i \ \text{Sin} \propto ; V_i = \text{RMS value of supply voltage.}$$

Current after the thyristor turns on for a resistive load is

$$I_{ON} = V_{ON} / R = \sqrt{2}\ V_i / R \ \text{Sin} \propto$$

Neglecting delay and spread time and assuming linear variation of voltage and current during turn on

$$V_{ak} = \sqrt{2}\ V_i \text{Sin} \propto \left(1 - t / t_{ON}\right). \text{ where } V_H \text{ has been neglected.}$$

$$i_a = \frac{\sqrt{2}\ V_i \text{Sin} \propto}{R} \ t / t_{ON}$$

$\therefore$ Total switching energy loss

$$E_{ON} = \int_o^{t_{ON}} v_{ak}\, i_a\, dt = \frac{2Vi^2}{R} \text{Sin}^2 \propto \int_o^{t_{ON}} \left(1 - t / t_{ON}\right) t / t_{ON}\ dt$$

$$= \frac{2Vi^2}{R} \text{Sin}^2 \propto \ \frac{t_{ON}}{2} \left(1 - \frac{2}{3}\right) = \frac{Vi^2}{3R} \text{Sin}^2 \propto t_{ON}$$

E_{ON} occurs once every cycle. If the supply frequency is f then average turn on power loss is given by.

$$P_{ON} = E_{ON} f = \frac{Vi^2}{3R} \text{Sin}^2 \propto t_{ON} f$$

(ii) If the firing angle is $\propto$ the thyristor conducts for π-$\propto$ angle. Instantaneous current through the device during this period is

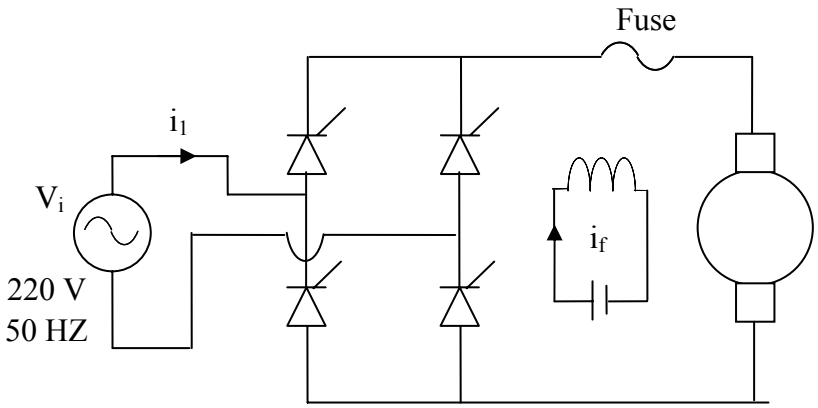
$$i_a = R \frac{\sqrt{2}\ V_i \text{Sin}\, \omega t}{R} \quad \propto \ < \omega t \leq \pi$$

Where t_{ON} & V_H have been neglected for simplicity.

$\therefore$ total conduction energy loss over one cycle is

$$E_C = \int_{\alpha/\omega}^{\pi/\omega} V_{ak}\, i_a\, dt = \frac{1}{\omega}\int_{\alpha}^{\pi} V_H \frac{\sqrt{2}\, V_i}{R} \sin\theta\, d\theta = \frac{\sqrt{2}\, V_i\, V_H}{\omega R}\left(1+\cos\alpha\right)$$

$$\therefore \text{ Average conduction power loss } = P_C = E_c f = \frac{\sqrt{2}\, V_i\, V_H}{2\pi R}\left(1+\cos\alpha\right)$$



3. In the ideal single phase fully controlled converter T_1 & T_2 are fired at a firing angle α after the positive going zero crossing of V_i while T_3 & T_4 are fired α angle after the negative going zero crossing of V_i, If all thyristors have a turn off time of 100 μs, find out maximum allowable value of α.

Answer: As T_1 & T_2 are fired at an angle α after positive going zero crossing of V_i, T_3 & T_4 are subjected to a negative voltage of $-V_i$. Since this voltage remain negative for a duration (π-α) angle (after which $-V_i$ becomes positive) for safe commutation $(\pi - \text{Max}) \geq \omega t_{off}$ $\therefore$ $\alpha_{Max} = 178.2^0$.

4.7 The Triac

The Triac is a member of the thyristor family. But unlike a thyristor which conducts only in one direction (from anode to cathode) a triac can conduct in both directions. Thus a triac is similar to two back to back (anti parallel) connected thyristosr but with only three terminals. As in the case of a thyristor, the conduction of a triac is initiated by injecting a current pulse into the gate terminal. The gate looses control over conduction once the triac is turned on. The triac turns off only when the current through the main terminals become zero. Therefore, a triac can be categorized as a minority carrier, a bidirectional semi-controlled device. They are extensively used in residential lamp dimmers, heater control and for speed control of small single phase series and induction motors.

4.7.1 Construction and operating principle

Fig. 4.12 (a) and (b) show the circuit symbol and schematic cross section of a triac respective. As the Triac can conduct in both the directions the terms “anode” and “cathode” are not used for Triacs. The three terminals are marked as MT_1 (Main Terminal 1), MT_2 (Main Terminal 2) and the gate by G. As shown in Fig 4.12 (b) the gate terminal is near MT_1 and is connected to both

N_3 and P_2 regions by metallic contact. Similarly MT_1 is connected to N_2 and P_2 regions while MT_2 is connected to N_4 and P_1 regions.

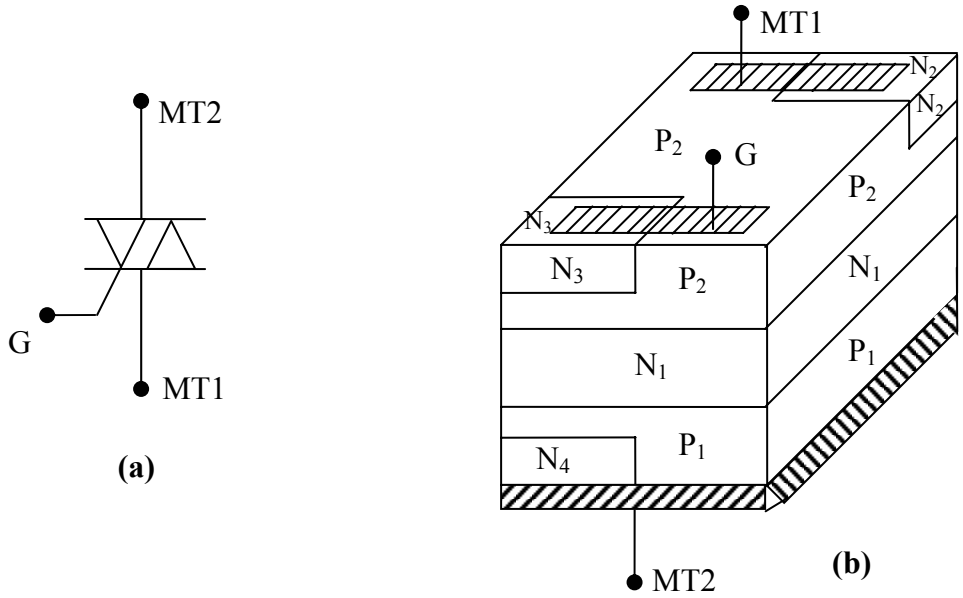


Fig. 4.12: Circuit symbol and schematic construction of a Triac
(a) Circuit symbol (b) Schematic construction.

Since a Triac is a bidirectional device and can have its terminals at various combinations of positive and negative voltages, there are four possible electrode potential combinations as given below

1. MT_2 positive with respect to MT_1, G positive with respect to MT_1
2. MT_2 positive with respect to MT_1, G negative with respect to MT_1
3. MT_2 negative with respect to MT_1, G negative with respect to MT_1
4. MT_2 negative with respect to MT_1, G positive with respect to MT_1

The triggering sensitivity is highest with the combinations 1 and 3 and are generally used. However, for bidirectional control and uniforms gate trigger mode sometimes trigger modes 2 and 3 are used. Trigger mode 4 is usually averded. Fig 4.13 (a) and (b) explain the conduction mechanism of a triac in trigger modes 1 & 3 respectively.

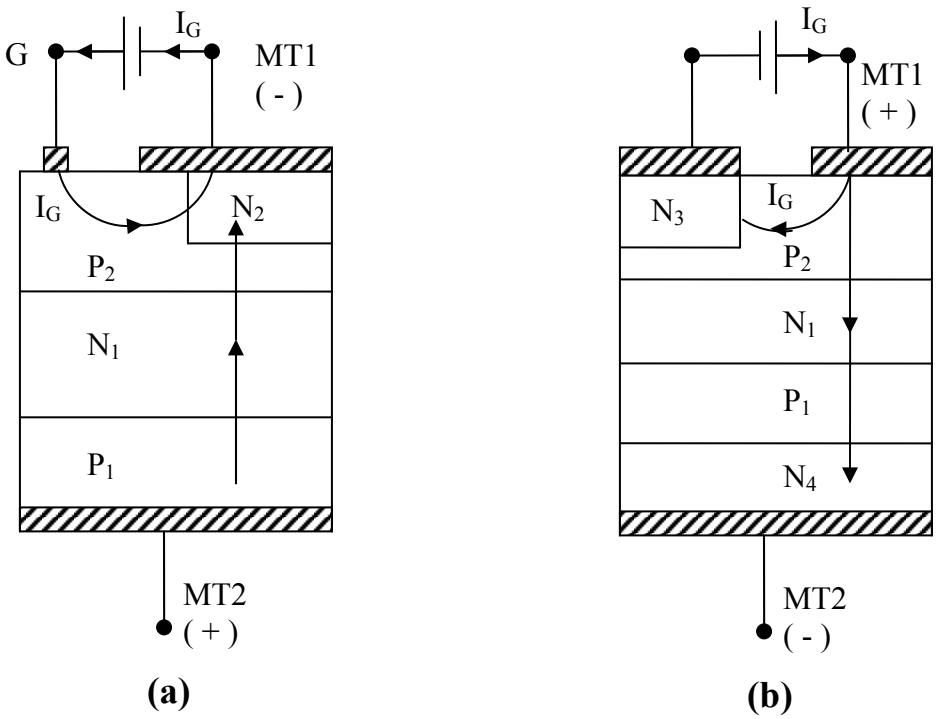


Fig. 4.13: Conduction mechanism of a triac in trigger modes 1 and 3
(a) Mode – 1 , (b) Mode – 3 .

In trigger mode-1 the gate current flows mainly through the P_2 N_2 junction like an ordinary thyristor. When the gate current has injected sufficient charge into P_2 layer the triac starts conducting through the P_1 N_1 P_2 N_2 layers like an ordinary thyristor.

In the trigger mode-3 the gate current I_g forward biases the P_2 P_3 junction and a large number of electrons are introduced in the P_2 region by N_3. Finally the structure P_2 N_1 P_1 N_4 turns on completely.

4.7.2 Steady State Output Characteristics and Ratings of a Triac

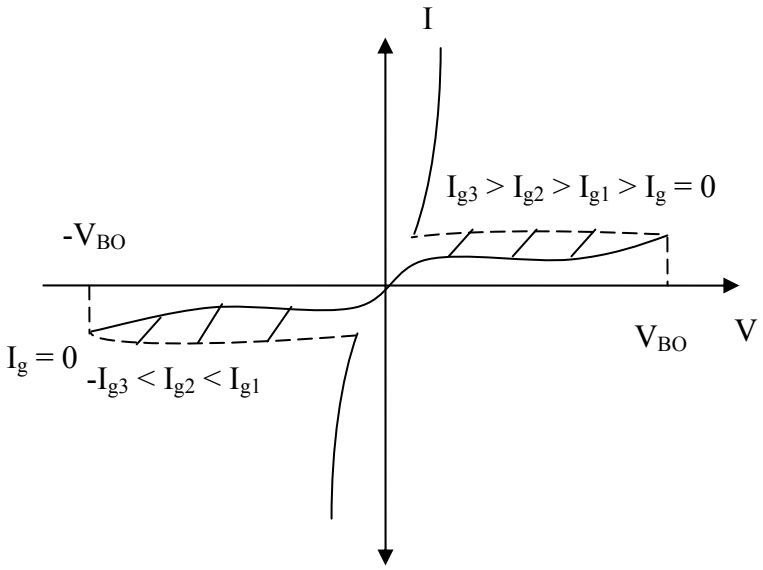


Fig. 4.14: Steady state V – I characteristics of a Triac

From a functional point of view a triac is similar to two thyristors connected in anti parallel. Therefore, it is expected that the V-I characteristics of Triac in the 1st and 3rd quadrant of the V-I plane will be similar to the forward characteristics of a thyristors. As shown in Fig. 4.14, with no signal to the gate the triac will block both half cycle of the applied ac voltage provided its peak value is lower than the break over voltage (V_{BO}) of the device. However, the turning on of the triac can be controlled by applying the gate trigger pulse at the desired instance. Mode-1 triggering is used in the first quadrant where as Mode-3 triggering is used in the third quadrant. As such, most of the thyristor characteristics apply to the triac (ie, latching and holding current). However, in a triac the two conducting paths (from MT_1 to MT_2 or from MT_1 to MT_1) interact with each other in the structure of the triac. Therefore, the voltage, current and frequency ratings of triacs are considerably lower than thyristors. At present triacs with voltage and current ratings of 1200V and 300A (rms) are available. Triacs also have a larger on state voltage drop compared to a thyristor. Manufacturers usually specify characteristics curves relating rms device current and maximum allowable case temperature as shown in Fig 4.15. Curves relating the device dissipation and RMS on state current are also provided for different conduction angles.

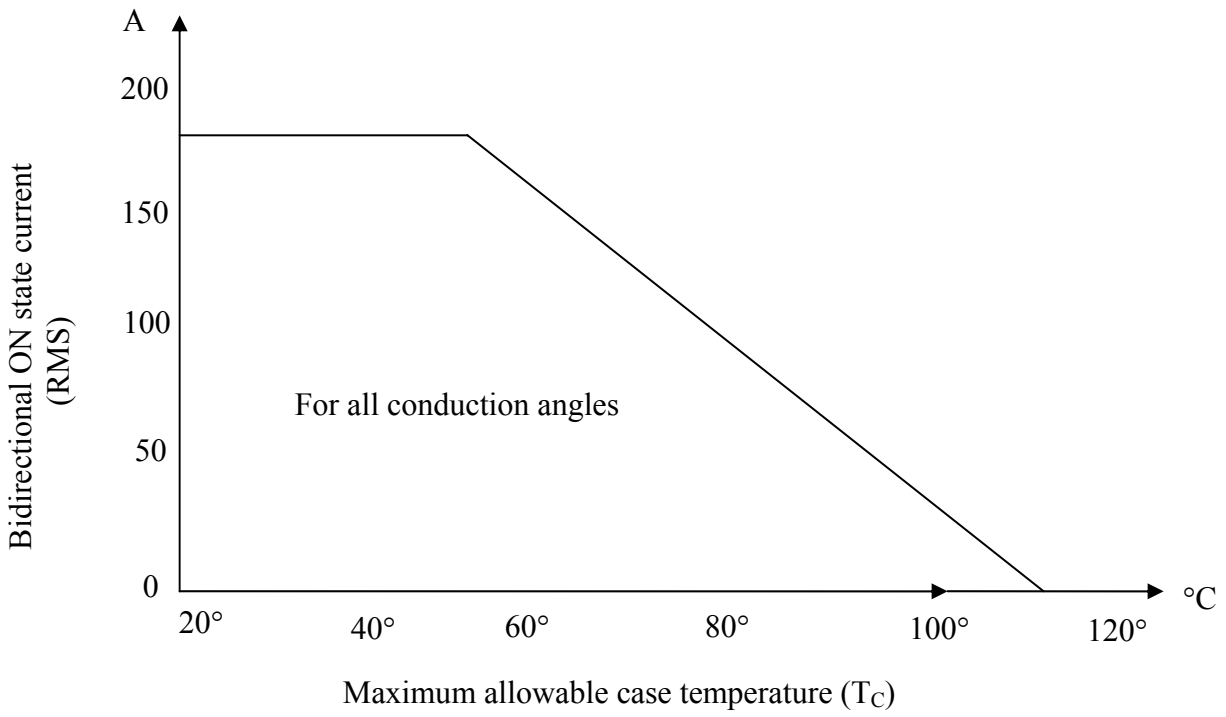


Fig. 4.15: RMS ON state current Vs maximum case temperature.

4.7.3 Triac Switching and gate trigger circuit

Unlike a thyristor a triac gets limited time to turn off due to bidirectional conduction. As a result the triacs are operated only at power frequency. Switching characteristics of a triac is similar to that of a thyristor. However, turn off of a triac is extremely sensitive to temperature variation and may not turn off at all if the junction temperature exceeds certain limit. Problem may arise when a triac is used to control a lagging power factor load. At the current zero instant (when the triac turns off) a reverse voltage will appear across the triac since the supply voltage is negative at that instant. The rate of rise of this voltage is restricted by the triac junction capacitance only. The resulting dv/dt may turn on the triac again. Similar problem occurs when a triac is used to control the power to a resistive element which has a very low resistance before normal working condition is reached. If such a load (e.g. incandescent filament lamp) is switch on at full supply voltage very large junction capacitance charging current will turn ON the device. To prevent such condition an R-C snubber is generally used across a triac.

The triac should be triggered carefully to ensure safe operation. For phase control application, the triac is switched on and off in synchronism with the mains supply so that only a part of each half cycle is applied across the load. To ensure 'clean turn ON' the trigger signal must rise rapidly to provide the necessary charge. A rise time of about 1 μs will be desirable. Such a triac gate triggering circuit using a "diac" and an R-C timing network is shown in Fig 4.16.

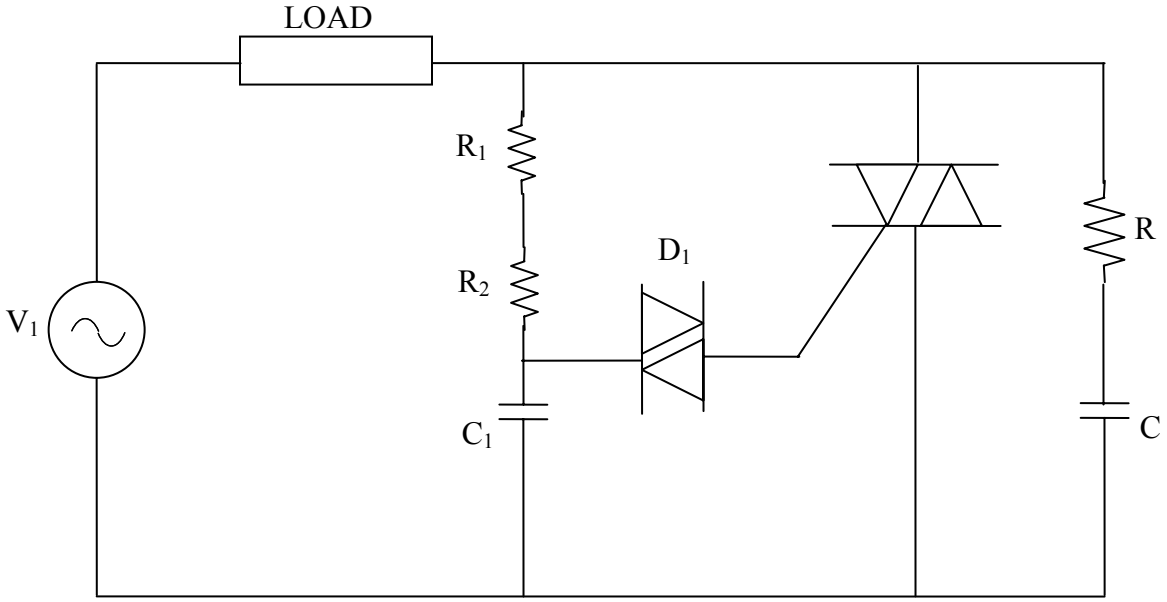


Fig. 4.16: Triac triggering circuit using a diac.

In this circuit as Vi increases voltage across C_1 increases due to current flowing through load, R_1, R_2 and C_1. The voltage drop across diac D_1 increases until it reaches its break over point. As D_1 conducts a large current pulse is injected into the gate of the triac. By varying R_2 the firing can be controlled from zero to virtually 100%.

Exercise 4.5

1) Fill in the blank(s) with the appropriate word(s)

i. A Triac is a _____ minority carrier device

ii. A Triac behaves like two _____ connected thyristors.

iii. The gate sensitivity of a triac is maximum when the gate is _____ with respect to MT_1 while MT_2 is positive with respect to MT_1 or the gate is _____ with respect to MT_1 while MT_2 is negative with respect to MT_1

iv. A Triac operates either in the _____ or the _____ quadrant of the i-v characteristics.

v. In the _____ quadrant the triac is fired with _____ gate current while in the _____ quadrant the gate current should be _____.

vi. The maximum possible voltage and current rating of a Triac is considerably _____ compared to thyristor due to _____ of the two current carrying paths inside the structure of the triac.

vii. To avoid unwanted turn on of a triac due to large dv/dt _____ are used across triacs.

viii. For "clean turn ON" of a triac the _____ of the gate current pulse should be as _____ as possible.

Answer: (i) bidirectional; (ii) anti parallel; (iii) positive, negative; (iv) first, third; (v) first, positive, third, negative (vi) lower, interaction; (vii) R-C shubbers; (viii) rise time, small.

References

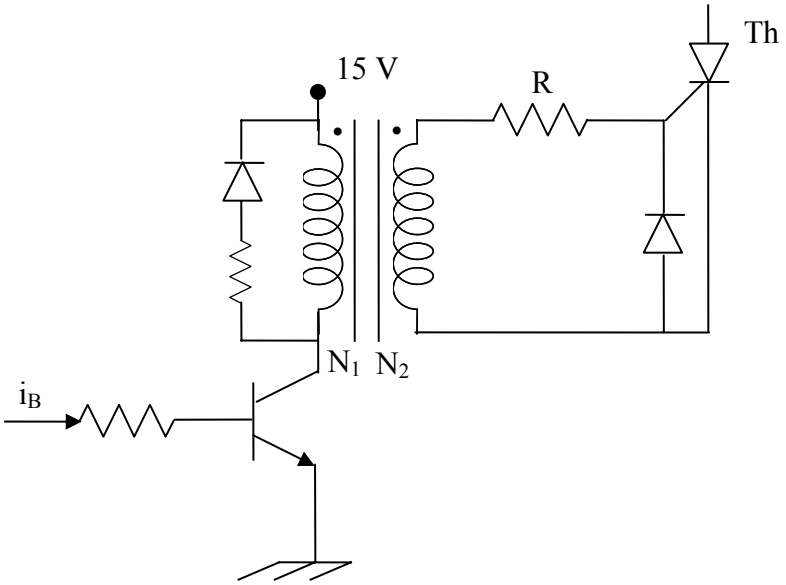
1. Dr. P.C. Sen, “Power Electronics”; Tata McGrow Hill Publishing Company Limited; New Delhi.
2. Dr. P.S. Bimbhra, “Power Electronics” Khanna Publishers

Lesson Summary

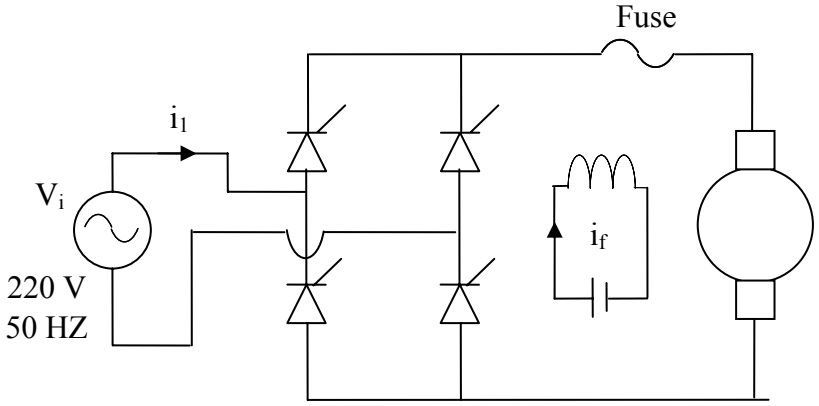
- Thyristor is a four layer, three terminal, minority carrier, semi-controlled device.
- The three terminals of a thyristor are called the anode, the cathode and the gate.
- A thyristor can be turned on by increasing the voltage of the anode with respect to the cathode beyond a specified voltage called the forward break over voltage.
- A thyristor can also be turned on by injecting a current pulse into the gate terminal when the anode voltage is positive with respect to the cathode. This is called gate triggering.
- A thyristor can block voltage of both polarity but conducts current only from anode to cathode.
- After a thyristor turns on the gate looses control. It can be turned off only by bringing the anode current below holding current.
- After turn on the voltage across the thyristor drops to a very low value (around 1 volt). In the reverse direction a thyristor blocks voltage up to reverse break down voltage.
- A thyristor has a very low conduction voltage drop but large switching times. For this reason thyristors are preferred for high power, low frequency line commutated application.
- A thyristor is turned off by bringing the anode current below holding current and simultaneously applying a negative voltage (cathode positive with respect to anode) for a minimum time called “turn off time”.
- A triac is functionally equivalent to two anti parallel connected thyristors. It can block voltages in both directions and conduct current in both directions.
- A triac has three terminals like a thyristor. It can be turned on in either half cycle by either a positive on a negative current pulse at the gate terminal.
- Triacs are extensively used at power frequency ac load (eg heater, light, motors) control applications.

Practice Problems and Answers

1. Explain the effect of increasing the magnitude of the gate current and junction temperature on (i) forward and reverse break down voltages, (ii) forward and reverse leakage currents.

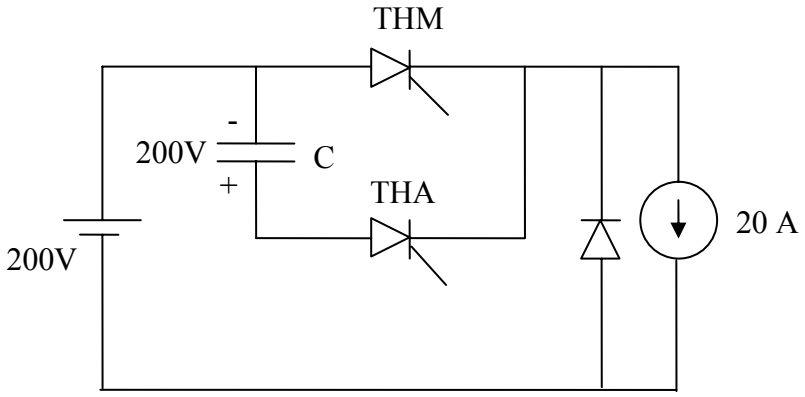


2. The thyristor Th is triggered using the pulse transformer shown in figure. The pulse transformer operates at 10 KHZ with a duty cycle of 40%. The thyristor has maximum average gate power dissipation limit of 0.5 watts and a maximum allow able gate voltage limit of 10 volts. Assuming ideal pulse transformer, find out the turns ratio N_1/N_2 and the value of R.



3. A thyristor full bridge converter is used to drive a dc motor as shown in the figure. The thyristors are fired at a firing angle $\propto = 0°$ when motor runs at rated speed. The motor has on armature resistance of 0.2 Ω and negligible armature inductance. Find out the peak surge current rating of the thyristors such that they are not damaged due to sudden loss of field excitation to the motor. The protective fuse in series with the motor is designed to disconnect the motor within $\frac{1}{2}$ cycle of fault. Find out the $\int i^2 dt$ rating of the thyristors.
4. Why is it necessary to maximize the peripheral contact area of the gate and the cathode regions? A thyristor used to control the voltage applied to a load resistance from a 220v,

50HZ single phase ac supply has a maximum di_a/dt rating of 50 A / μs. Find out the value of the di_a/dt limiting inductor to be connected in series with the load resistance.



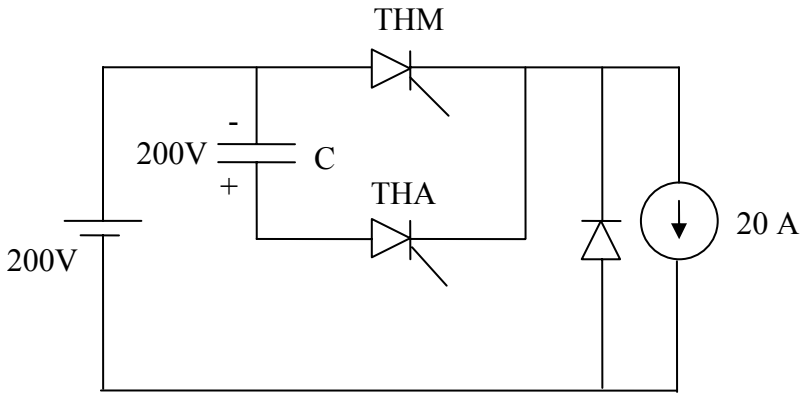
5. In a voltage commutated dc – dc thyristor chopper the main thyristor THM is commutated by connecting a pre-charged capacitor directly across it through the auxiliary thyristor THA as shown in the figure. The main thyristor THM has a turn off time off 50μs and maximum dv/dt rating of 500v/ μs. Find out a suitable value of C for safe commutation of THM.

Answers to Practice Problems

1.

i. Forward break down voltage reduces with increasing gate current. It increases with junction temperature up to certain value of the junction temperature and then falls rapidly with any further increase in temperature.
Reverse break down voltage is independent of the gate current magnitude but decreases with increasing junction temperature.

ii. Forward leakage current is independent of the gate current magnitude but increases with junction temperature.
Reverse leakage current increases with both the junction temperature and the magnitude of the gate current.



2. Figure shows the equivalent gate drive circuit of the thyristor. For this circuit one can write

$$E = R\,i_g + V_g \quad \text{OR} \quad V_g = E - R\,i_g$$

The diode D clamps the gate voltage to zero when E goes negative.

Now for $i_g = O$, $V_g = E$. Since $V_g\big|_{Max} = 10$ v $E = 10$ v

But $E = {}^{N_2}\!/_{N_1}\,15$ $\therefore$ ${}^{N_2}\!/_{N_1} = {}^{15}\!/_{10} = 1.5$

Gate pulse width = 0.4×10^{-4} Sec = 40μs. <100μs.

$\therefore$ instantaneous gate power dissipation limit can be used.

$$\therefore \quad V_g i_g\big|_{Max} = \frac{P_{av}\big|_{Max}}{\delta} = \frac{0.2}{0.4} = 0.5 \text{ watts}$$

For maximum utilization of the gate power dissipation limit the gate load line ie $V_g = E - i_g R = 10 - i_g R$ should be tangent to the maximum power dissipation curve $V_g\, i_g = 0.5$

Let the operating V_g and i_g be V_{go} & i_{go}

$$\therefore \quad V_{go} = 10 - i_{go} R$$
$$V_{go}\, i_{go} = 0.5$$
$$\therefore\ i_{go}^2 R - 10\, i_{go} + 0.5 = 0$$

Since $V_g = 10 - i_g R$ is tangent to $V_g i_g = 0.5$ at V_{go}, i_{go}.

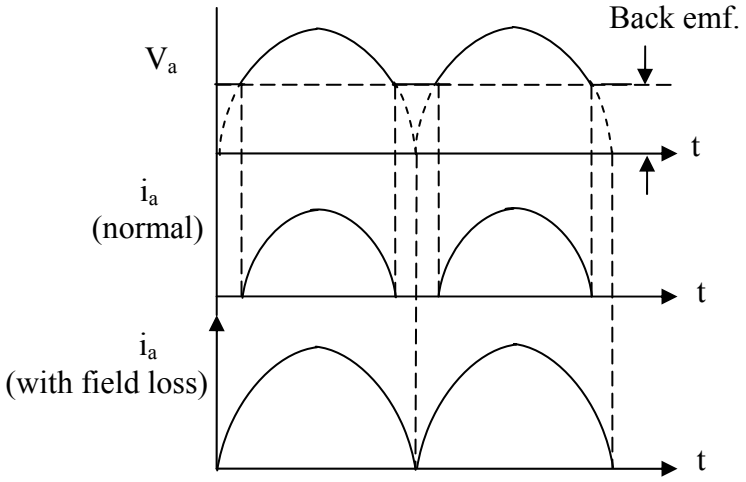
Slope of the tangent of $V_g i_g = 0.5$ at $(V_{go}, i_{go}) = -R$

$$\therefore \; -R = \left.\frac{dv_g}{di_g}\right|_{(v_{go},i_{go})} = \left.\frac{-v_g}{i_g}\right|_{(v_{go},i_{go})} = -\frac{v_{go}}{i_{go}}$$

$$\therefore \; R = \frac{v_{go}}{i_{go}} = \frac{v_{go}\, i_{go}}{i_{go}^{\,2}} = \frac{0.5}{i_{go}^{\,2}}$$

$$\therefore \; i_{go}^{\,2} \times \frac{0.5}{i_{go}^{\,2}} - 10 i_{go} + 0.5 = 0 \quad \text{or} \quad 10 i_{go} = 1 \quad \text{or} \quad i_{go} = 0.1$$

$$\therefore \; R = 0.5 \Big/ i_{go}^{\,2} = \frac{0.5}{.01} = 50\,\Omega$$



3. Figure shows the armature voltage (firm line) and armature current of the motor under normal operating condition at rated speed. If there is a sudden loss of field excitation back emf will become zero and armature current will be limited solely by the armature resistance.

The peak magnitude of the fault current will be $\frac{220\sqrt{2}}{.2} = 1556(\text{Amps})$.

It the thyristors have to survive this fault at least for $1/2$ cycle (after which the fuse blows) $I_{sM} >$ 1556 Amps.

The fuse blows within $1/2$ cycle of the fault occurring. Therefore the thyristors must withstand the fault for at least $1/2$ cycle.

Therefore, the i^2t rating of the thyristor should be

$$\int i^2\,dt = \int_0^{10^{-2}} \left(1556 \sin 100\pi t\right)^2$$

$$= \frac{(1556)^2}{2} \int_0^{10^{-2}} \left[1 - \cos 200\pi t\right] dt$$

$$= \tfrac{1}{2} \times 10^{-2} (1556)^2 = 1.21 \times 10^4 \text{ A}^2 \text{ Sec}$$

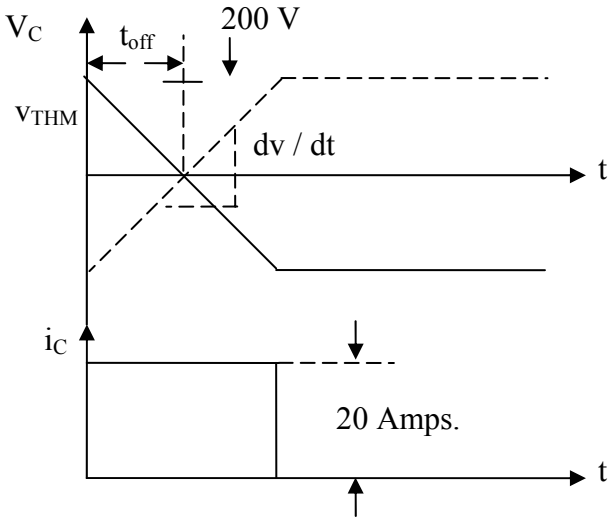
4. At the beginning of the turn on process the thyristor starts conducting through the area adjacent to the gate. This area spreads at a finite speed. However, if rate of increase of anode current is lager than the rate of increase of the current conduction are, the current density increases with time. This may lead to thyristor failure due to excessive local heating. However, if the contact area between the gate and the cathode is large a thyristor will be able to handle a relatively large di_a/dt without being damaged.

The maximum di_a/dt will occur when the thyristor is triggered at $\propto = 90°$. Then

$$L \frac{di_a}{dt} = \sqrt{2} \times 220 \sin 90^0$$

Since $di_a/dt\big|_{Max} = 50 \times 10^6 \text{ A / Sec}$

$$L\Big|_{min} = \frac{\sqrt{2} \times 220}{\left(di_a/dt\right)_{Max}} = 6.22 \times 10^{-6} \text{ H} = 6.22\,\mu\text{H}$$



5. As soon as THA is turned on the load current transfer from THM to C. the voltage across THM is the negative of the capacitance voltage. Figure shows the waveforms of voltage across the capacitor (v_c), voltage across the main thyristor (V_{THM}) and the capacitor current i_c. From figure $\frac{dv}{dt} = i_c / c$

Now $i_c = 20$ Amps & $\left.\frac{dv}{dt}\right|_{Max} = 500\ v/\mu s$

$$\therefore\ C\Big|_{Min} = \frac{i_c}{\left.\frac{dv}{dt}\right|_{Max}} = \frac{20}{500\times10^{6}} = 4\times10^{-8}\,F = 0.04\,\mu F$$

The circuit turn off time is the time taken by the capacitor voltage to reach zero from an initial value of 200v. This time must be greater than the turn off time of the device.

Now $C\frac{dv_c}{dt} = i_c = 20$

$$\therefore\ \Delta v_c = \frac{20\times\Delta t}{c} \qquad \Delta v = 200 - 0 = 200$$

$$\Delta t = t_{off}$$

$$\therefore\ 200 = \frac{20\times50\times10^{-6}}{C}$$

$$\therefore\ C = \frac{20\times50\times10^{-6}}{200} = 5\ \mu F$$

For safe commutation of THM the higher value of C must the chosen

$\therefore$ the required value of C = 5 μF.

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