

SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, Bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

- i) Switches using overdriven Emitter Followers.
- ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.
- iii) CMOS switch for Multiplying type DACs .
- iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have a offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q1(NPN) and Q2(PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When $V_B1 = V_B2 = +5.75V$, Q1 is in saturation and Q2 is OFF. And $V_E \approx 5V$ with

$$V_{BE1} = V_{BE2} = 0.75V$$

Case 2:

When $V_B1 = V_B2 = -5.75V$, Q2 is in saturation and Q1 is OFF. And $V_E \approx -5V$ with

$$V_{BE1} = V_{BE2} = 0.75V$$

Thus the terminal B of the resistor R_E is connected to either -5V or +5V depending on the input bit.

Switches using MOS transistor:

- i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp. The complementary outputs Q and \bar{Q} drive the gates of the MOSFET M1 and M2 respectively. The SR flipflop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with $S=1$ and $R=0$ makes $Q=1$ and $\bar{Q}=0$. This makes the transistor M1 ON, thereby connecting the resistor R to reference voltage $-VR$. The transistor M2 remains in OFF condition.

Case 2:

When the bit line is 0 with $S=0$ and $R=1$ makes $Q=0$ and $\bar{Q}=1$. This makes the transistor M2 ON, thereby connecting the resistor R to Ground. The transistor M1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with a very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line \bar{Q} is low, M1 becomes ON connecting VR to the non-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line \bar{Q} is high, M2 becomes ON connecting Ground to the non-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M1 and M2. The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M1 and M2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M1 is ON and M2 is OFF. Thus current IK is diverted to $I_{O'}$ bus.

Case 2:

When the logic input is 0, M2 is ON and M1 is OFF. Thus current IK is diverted to I_O bus.

CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of $VR - VTH$ and PMOS transistor passing minimum voltage of VTH). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from VR to $0V$ acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

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