SUB THRESHOLD CURRENT

The sub threshold current always flows from source to drain even if the gate to source voltage is lesser than the threshold voltage of the device. This happens due to the carrier diffusion between the source and drain regions of the CMOS transistor in weak inversion. When gate to source voltage is smaller than but very close to threshold voltage of the device then sub threshold current becomes significant.

As observed by [4] currently, sub threshold leakage is still playing the main part in the three mechanisms. However, researchers believe that gate leakage and reverse-biased junction Band To Band Tunneling (BTBT) will be as important as sub threshold from 45 nm process downwards. In addition, with technology scaling, the gate oxide thickness will be reduced and the substrate doping densities will be increased. As a result other factors such as gate-induced drain leakage (GIDL) and drain-induced barrier lowering (DIBL) will also become more and more evident. Therefore, future effective low leakage design will need to target at several components since all of them play an important role in the total leakage consumption. Various techniques at process and circuit level exist to reduce leakage consumption, including modifying doping profile, oxide thickness and channel length. Forward or inverse body biasing is also one of them, which is a technique resulting in variable threshold CMOS.

Sub threshold current *Isub*, which occurs when gate voltage is below threshold voltage *Vth*, is a main part of leakage current [2]. *Isub* depends on different effects and voltages, which are formulated in following equations [1]:

$$I_{sub} = I_0 \cdot e^{\frac{q}{nk_BT}(V_{gs} - V_{th0} + \gamma V_{bs} + \eta V_{ds})} \left(1 - e^{\frac{-qV_{ds}}{k_BT}}\right) \quad (1)$$

$$I_0 = \mu \cdot \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si} NDEP}{2\Phi_S}} \left(\frac{k_BT}{q}\right)^2 \quad (2)$$

$$\eta \approx \frac{-0.5 \cdot (ETA0 + ETAB \cdot V_{bs})}{cosh\left(DSUB \frac{L_{eff}}{\sqrt{\frac{\varepsilon_{Si}^{3/2}}{\varepsilon_{ox}\sqrt{q}}} \cdot \sqrt{\frac{T_{ox}}{\sqrt{NDEP}}}}\right) - 1} \quad (3)$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}}}{\varepsilon_{ox}} \cdot \sqrt{NSUB} \cdot T_{ox} \quad (4)$$

$$T_d = \frac{k' \cdot V_{dd} C_L}{(W/L) \cdot (V_{dd} - V_{th})^{\alpha}} \quad (5)$$

Where

q is the electrical charge.

T is the temperature,

n is the sub threshold swing coefficient,

kB is the Boltzmann constant,

η is the drain induced barrier lowering (DIBL) coefficient,

γ is the body effect coefficient,

μ is the mobility,

Vth0 is the zero-bias threshold voltage,

Vgs is the gate-source voltage,

Vbs is the bulk-source voltage,

Vds is the drain-source voltage,

εox and *εSi* are the gate dielectric constants of gate oxide and silicium,

NSUB is the uniform substrate doping concentration and

NDEP the channel doping concentration,

Tox is the thickness of the oxide layer,

ΦS is the surface potential,

DSUB and *ETA0* are technology dependent DIBL coefficients, and

ETAB is a body-bias coefficient of the BSIM4-Modell.

The delay *Td* of a CMOS device can be approximated by equation (5).

Where

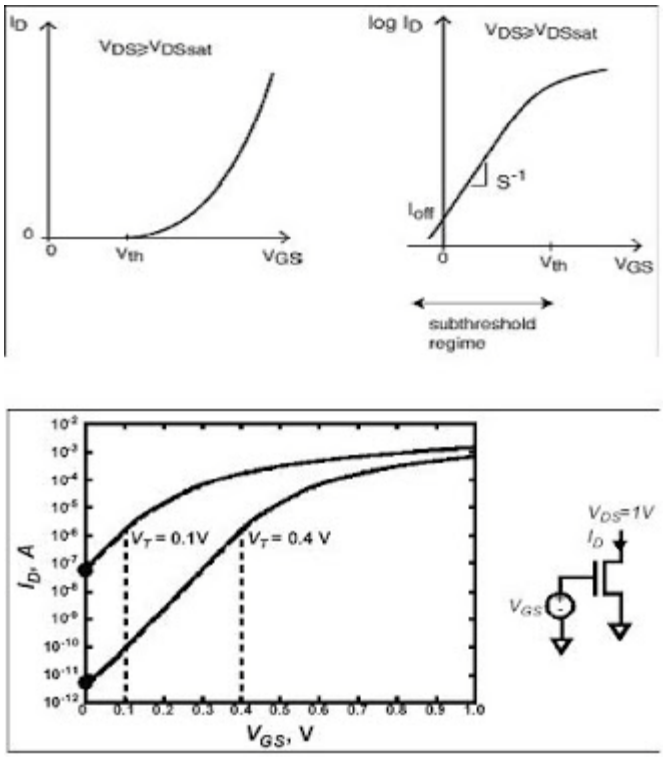
k' is a technology constant,

CL is the load, and

α models the short channel effects [3].

Variation of Vth is a common technique to reduce leakage because Isub exponentially scales with Vth (see Equation 1). Thus, higher Vth results in lower leakage. However, from equation (5) follows higher Vth additionally results in longer delay [2]. Hence, optimize the design with the balance application of low Vth (LVT) and high Vth devices (HVT).

Transfer characteristics of MOSFET for VGS near Vth are shown in below figure.



Transfer characteristics of MOSFET V_{GS} near Vth [2]

From the above figure it can be observed that I_D increases exponentially with reduction in Vth.

- If $V_{DS} = 0 \Rightarrow I_{sub} = 0$
- If $V_{DS} >> nv_T \Rightarrow I_{sub} = \frac{W}{L}\mu_e v_T^2 C_{sth} e^{\frac{V_{GS}-V_{th}}{nv_T}}$
- With $n = 1 + \frac{\gamma}{2\sqrt{2\Phi_f}} = 1 + \frac{C_{sth}}{C_{ox}}$

$$W_{off} = I_{off} V_{DD}$$

As noted by [4] key dependencies of the sub threshold slope can be summarized as follows:

- *Tox* ↓ =>*Cox* ↑=> *n* ↓ =>sharper sub threshold

- *NA* ↑ =>*Csth* ↑ =>*n* ↑ =>softer sub threshold

- *VSB* ↑ =>*Csth* ↓ =>*n* ↓ =>sharper sub threshold

- *T* ↑ =>softer sub threshold

How to minimize sub threshold leakage?

A increase in the threshold voltage of the device keeps the Vgs of the NMOS transistor safely below the Vt,n. This is the case for logic zero input. For the logic one input increase in the threshold voltage of the device keeps the |Vgs| of the PMOS transistor safely below the |Vt,p|.

Source : http://asic-soc.blogspot.in/2008/04/sub-threshold-current.html